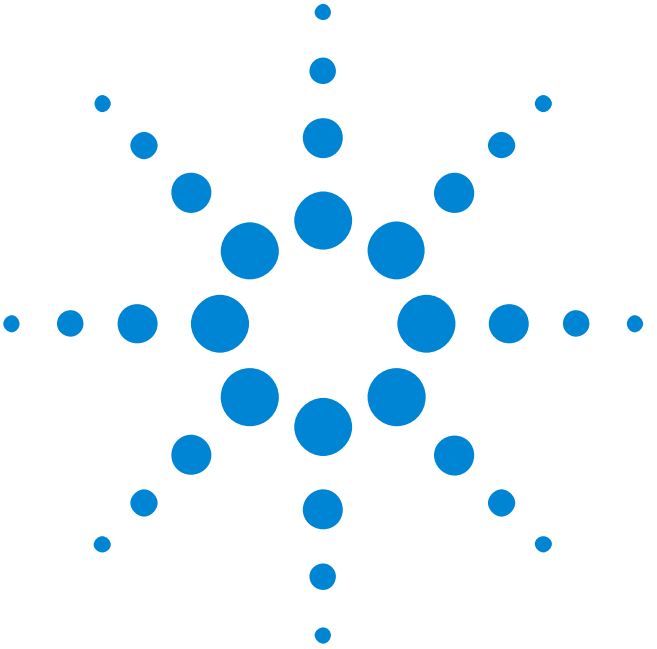

System Reference

Agilent Technologies

System Reference

Agilent 93000 SOC P–Series and C–Series

Agilent Technologies GmbH
SOC Business Unit

Agilent Part No. E7050-91017

Revision 3.0, January 2001

Legal Notice

Subject Matter

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Printing History

New editions are complete revisions of the guide reflecting alterations in the functionality of the instrument. Updates are occasionally made to the guide between editions. The date on the title page changes when an updated guide is published. To find out the current revision of the guide, or to purchase an updated guide, contact your Agilent Technologies representative.

Control Serial Number: First Edition applies directly to all instruments.

Preface

Objectives of this Manual

The manual provides information about the properties of the specific test system hardware of the Agilent 93000 SOC Series.

Audience

The manual is intended for engineers on the testfloor (test engineers, production engineers, manufacturing engineers).

Scope of the Manual

The manual covers feature-oriented reference material, capabilities, restrictions and other considerations regarding

- Test system components
- System start-up and shutdown
- DUT board design
  (mechanical and performance considerations)
- Device power supply
- Analog modules

Safety Information

The following general safety precautions must be observed during all phases of operation, service, and repair of this system. Failure to comply with these precautions or with specific warnings in this manual, violates safety standards and the intended use of the system. Agilent Technologies assumes no liability for the customer's failure to comply with these requirements.

This is a Safety Class 1 instrument (provided with terminals for protective grounding) and has been manufactured and tested according to international safety standards.

Operation

Please observe the following:

- Do not remove system covers when operating.
- Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.
- Capacitors inside the system may still be energized even if the system has been disconnected from its power source.

Warnings and Cautions

This manual uses warnings and cautions to denote hazards.

A **warning** calls attention to a procedure, practice or the like, which, if not correctly performed or adhered to, could result in injury or the loss of life. Do not proceed beyond a warning until the indicated conditions are fully understood and met.

A **caution** calls attention to a procedure, practice or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the equipment. Do not proceed beyond a caution until the indicated conditions are fully understood and met.

Table of Contents

Appendices

List Of Figures

1

System Overview

This chapter provides you with information on:

Revision History

Changes from Revision 1.0 (Aug. 99) to Revision 1.1 (Oct. 99)

The Chapter 6 *"Device PowerSupply"* on page 135 has been revised completely.

Changes from Revision 1.1 (Oct. 99) to Revision 2.0 (Dec. 99)

The Chapter 7 *"Analog Modules"* on page 183 has been added completely.

Changes from Revision 2.0 (Dec. 99) to Revision 2.1 (Apr. 00)

The Chapter 4 *"Test Head Filling and DUT Board Considerations"* on page 57 has been revised completely.

The Chapter 7 *"Analog Modules"* on page 183 has been revised for supporting the new analog modules completely.

Changes from Revision 2.1 (Apr. 00) to Revision 2.2 (Jun. 00)

A new section *"Master Clock System"* on page 49 has been added into *Chapter 3*.

The Chapter 4 *"Test Head Filling and DUT Board Considerations"* on page 57 has been revised completely.

The Chapter 6 *"Device PowerSupply"* on page 135 has been revised completely.

The section *"Synchronization"* on page 242 in *Chapter 7* has been revised.

Changes from Revision 2.2 (Jun. 00) to Revision 3.0 (Feb 01)

The Chapter 7 *"Analog Modules"* on page 183 has been revised for supporting the new analog module, General purpose TIA and for adding the parameter usages of TIA.

System Characterization

The Agilent 93000 SOC Series offers solutions for testing the entire range of most integrated Systems-on-a-Chip (SOC).

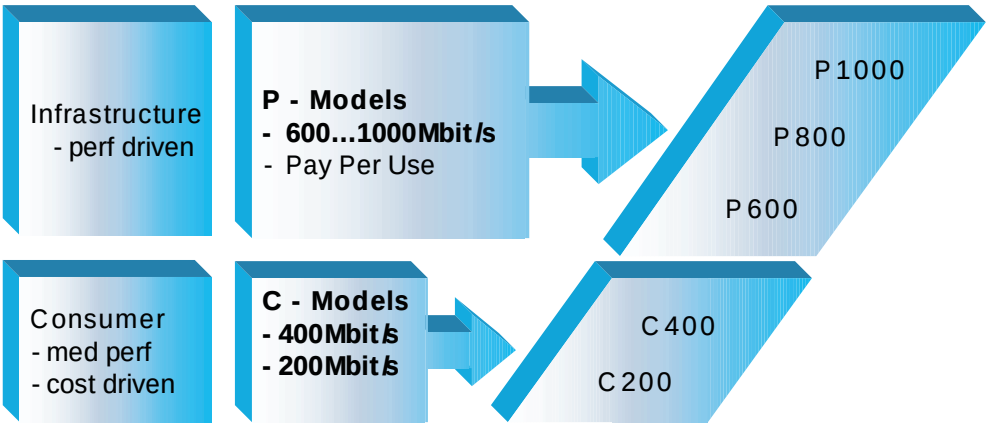


Figure 1 P- and C-Models of the Agilent 93000 SOC Series

The performance optimized models P1000, P800, and P600 are best suited in testing infrastructure devices. The cost-optimized models C400 and C200 use lower grade test processors for testing consumer applications. The model number indicates the maximum data rate in Gbit/s.

Compatibility

All models of the Agilent 93000 SOC Series are based on the same test processor technology and the same mechanical design. This is the basis for compatible test programs for the entire range of applications.

MACH-D Testing **Systems-on-a-Chip** (SOC devices) means having the capability and flexibility to effectively and comprehensively test *all* the functional components of an SOC. These functional areas include

- **M**emory
- **A**nalog
- **C**ommunications
- **H**igh-speed busses
- **D**igital complex

Addressing all these tester applications with one platform means dealing with two challenges:

1. Offering at-speed testing for highest speed devices combined with accurate analog test.
2. Enabling lowest cost-of-test (especially for manufacturing test of consumer-oriented devices).

Figure 2 The Agilent 93000 SOC Series Tester

Technical Highlights

Test Processor-Per-Pin Architecture

The technology required to address these challenges is a highly integrated Tester-on-a-Chip. The Test Processor-per-pin architecture combines all functions of the digital tester in one chip. This provides the foundation for full, fast and effective testing of all components integrated into SOC devices.

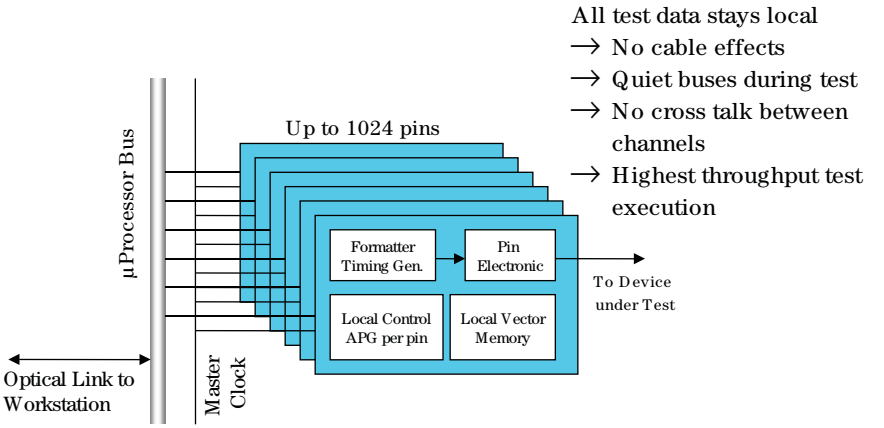


Figure 3 Test Processor-per-pin Architecture

Every pin in the Test Processor-per-pin architecture is its own tester.

System Architecture

The Agilent 93000 SOC Series testers combine highest speed digital test and highest precision analog measurement into a compact testhead.

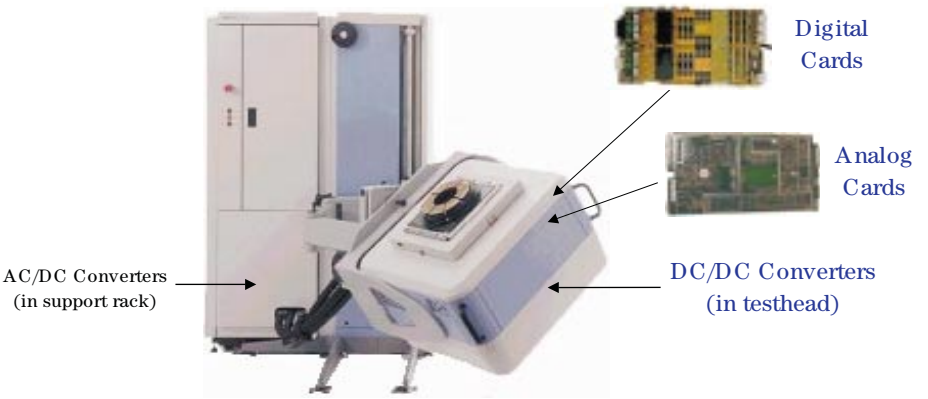


Figure 4 SOC System Integration

In order to achieve this high level of integration, all components are water-cooled. By keeping the junction temperature close to the stabilized water temperature, all components of the test system which are critical for accuracy operate under very narrow and well-defined conditions. This leads to minimized drift of all system parameters during the entire calibration interval and consequently to superior reliability.

More Highlights

More highlights of the SOC Series are:

- 112M vectors SDRAM vector memory
  Maximum of 256 k sequencer instructions SRAM. The sets containing your test data are also stored in the SRAM. This reduces the memory available for sequencer instructions. So the actual number of sequencer instructions you can store in the SRAM will be lower than the maximum of 256 k.
- 625 MHz maximum clock frequency
- Higher accuracy than the Agilent 83000 F-Series
- PMU per pin (parallel P/F results, and multiplexed value measurement per 16 pins)
- High Precision PMU per cardcage (128 pins)
- An active load per pin

- Maximum of 8 DPS boards (960 pins testhead) containing 4 DPS channels each
- Maximum of 8 blocks of 16 utility lines
- 6 general drive/receive edges on software level mapped to 8 hardware drive edges (4 of them have tristate capability) and 6 hardware receive edges
- Analog modules for high performance mixed-signal testing
  - High Resolution AWG (Arbitrary Waveform Generator)
  - High Speed AWG
  - Ultra High Speed AWG
  - High Resolution Digitizer
  - High Speed Digitizer
  - Dual High Speed Sampler
  - High Performance TIA (Time Interval Analyzer)
  - General purpose TIA(Time Interval Analyzer)

Major Components

The Agilent 93000 SOC Series test system consists of

- **Testhead** with DUT Interface (*"The Testhead"* on page 24)
- **Manipulator** for positioning the testhead (*"The Manipulator"* on page 26)
- **Support Rack** supplying the testhead with mains power, cooling water, and compressed air (*"The Support Rack"* on page 27)

Figure 5 SOC Series Model with 960 / 1024 Pins Testhead

These test system components are connected to:

- **Cooling system** (*"The Cooling System"* on page 28)
- **HP workstation** (*"The Workstation"* on page 29)

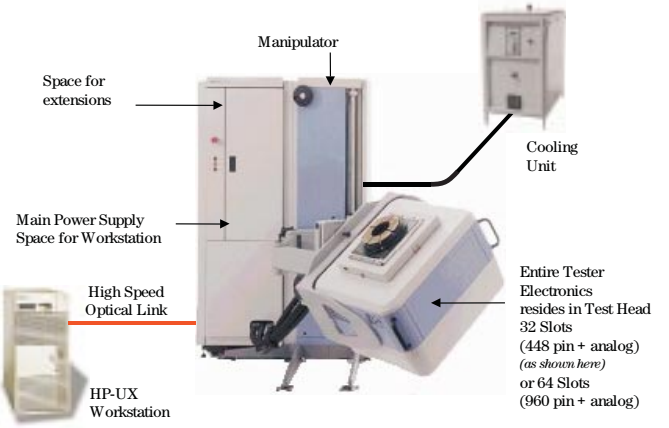


Figure 6 SOC Series Model with 448 Pins Testhead

The Testhead

The testhead is the heart of the system. It comprises all tester electronics and additional analog modules.

The Agilent 93000 SOC Series test system comes with a **960** pins/32 slots or a **448** pins/64 slots testhead, internally divided into *eight* resp. *four* cardcages. Each cardcage is a 128 pin module, powered separately by two DC/DC boards, and houses the channel boards and the optional device power supplies.

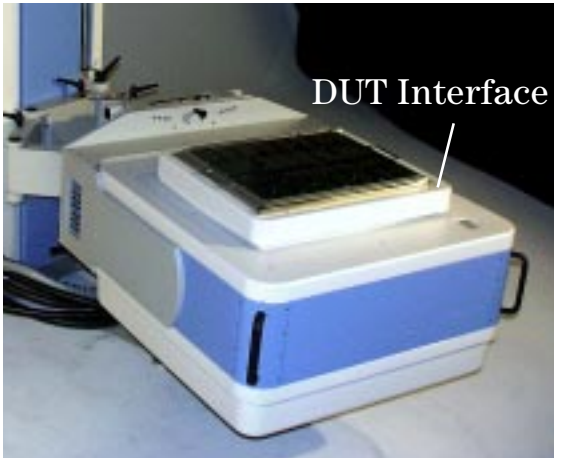


Figure 7 **Agilent 93000 SOC Series Testhead**

For detailed information on the tester electronics, refer to *"Tester Electronics"* on page 38.

For detailed information on the analog modules, refer to Chapter 7 *"Analog Modules"* on page 183.

DUT Interface

The device under test (DUT) is mounted on a DUT board which is connected to the I/O channels by the DUT interface. The DUT interface consists of high performance coax cabling and spring contact pins (pogo pins) which make the contact to the DUT board.

For details on DUT interfaces and boards, refer to Chapter 4 *"Test Head Filling and DUT Board Considerations"* on page 57.

Docking

The DUT interface provides docking capabilities to handlers and wafer probers. The docking mechanism is controlled by compressed air, but can also be operated manually, if required.

For detailed information on DUT board docking, refer to the *Docking Hardware Reference*.

Cooling

The testhead is water cooled. It receives its supply of cooling water from the support rack which in turn is connected by two flexible hoses to the cooling unit (refer to *"The Cooling System"* on page 28).

The Manipulator

The general-purpose manipulator supports and positions the testhead. It provides 6 degrees of freedom for the precise and repeatable connection between the testhead and handlers or wafer probers.

Figure 8 Manipulator

With the manipulator, the testhead can be moved horizontally and vertically, twisted and swung out sideways.

The vertical movement is usually controlled with a handheld remote control unit which controls a motor inside the manipulator, but can also be operated manually by using the manipulator crank.

For detailed information on testhead movement, refer to the *Docking Hardware Reference*.

The Support Rack

The support rack is attached to the manipulator. The support rack is the interface between the testhead and its primary supplies (mains power, cooling water, compressed air). The SOC Series can also have additional support racks (analog support racks) for installing additional analog instruments.

Figure 9 Support Rack

ON / OFF Unit

On the front panel of the support rack, the ON/OFF unit is situated, providing the ON button, the STANDBY button, the Emergency OFF button and an additional warning lamp.

For information on switching the tester on and off, refer to Chapter 2 *"System Startup"* on page 31.

Primary Power Box

The primary power box inside the support rack contains the connections to mains, the system's line switch, the line breaker, and individual breakers for the switched outlets, non/switched outlets, the auxiliary power supply and AC/DC converters.

AC / DC Converters

The AC/DC cardcage contains eight resp. four water and air cooled AC/DC converter boards which supply the testhead with 385 V DC. Each board supplies one cardcage.

The Cooling System

In order to achieve the SOC Series' high level of integration, all components are water-cooled. The water cooling not only keeps all important specifications stable but also avoids noisy fans in the testhead.

The 3rd-generation cooling system supplies cooling water to the support rack and to the testhead. It is powered by three-phase AC mains power.

Figure 10 Cooling Unit

The cooling system is connected to the support rack via four flexible water hoses. Another four flexible water hoses conduct the cooling water from the support rack to the testhead and from the testhead back to the support rack.

In order to adapt to various environments, Agilent Technologies offers two different kinds of cooling systems:

- The liquid/liquid Cooling Unit E2760D
- The liquid/air Chiller Unit E2759D

For detailed information on operation and control of the Cooling Unit resp. the Chiller Unit, refer to the *Cooling System Guide*.

The Workstation

The HP-UX workstation is the interface between the user and the Agilent 93000 SOC Series test system.

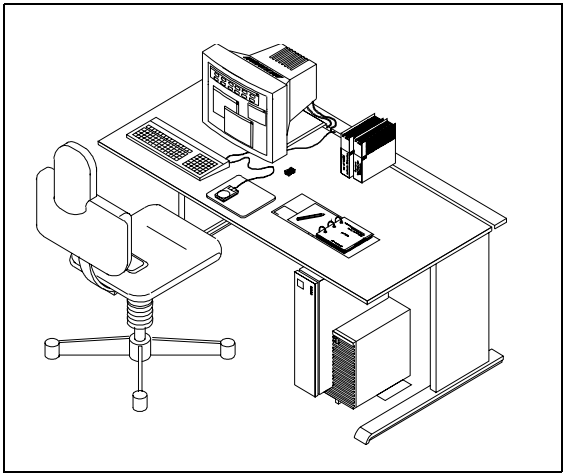


Figure 11 HP Workstation

SmarTest Software

The Agilent 93000 SOC Series SmarTest software runs on this workstation under the HP-UX operating system. SmarTest allows you to download setups and test data to the test system and to edit this data. All testing is carried out in the test system, and finally the results are read back by the workstation and displayed on the monitor.

During test program execution, upload and download are typically *not* necessary, since the test processors act independently from the workstation once the test program is started.

Diagnostics On the workstation, a diagnostic program can be run to check the system periodically or to identify the source of a problem.

2

System Startup

This chapter provides you with information on:

Switching the Tester On

The **ON/OFF Unit** is integrated in the front panel of the support rack. It provides illuminated ON/OFF buttons, an Emergency OFF button and an additional warning lamp.

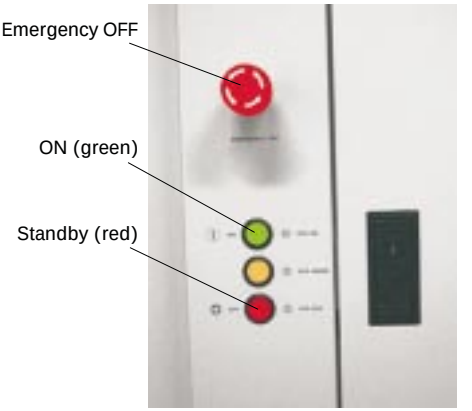


Figure 12 ON / OFF Switches on Support Rack Front Panel

Switching Procedure

To switch on the Agilent 93000 SOC Series test system:

1 Be sure the line switch at the rear of the support rack is in the ON position.

The line switch connects the power supply to mains and powers the rack interface board.

2 Press the ON button on the front panel.

Figure 13 ON Button

Green flashing (slow): The system starts cooling and connects mains to AC/DC converters and switched power outlets.

Green flashing (fast): The system starts DC/DC converters. Cooling is okay.

Green steadily lit: The system is up.

Warning Lamps

During the start-up procedure or when the system is running, the warning lamps indicate the following:

Yellow: Cooling warning when system is running

Red: The system has been shut down due to a failure. The unswitched power outlets and the auxiliary power supply are still connected to mains.

In these cases, inform the maintenance personnel.

Running the System Software

To start the SmarTest software, at the HP workstation type the following command at the HP-UX prompt:

```
hp93000 [-o]
```

The -o option starts the software in offline mode (hardware not connected).

The user interface windows appear on the screen.

For detailed information on starting up SmarTest, refer to the *Test Setup* manual (Part No. E7050-91010).

Shutting down

To shut down the system software, click the Quit push button in the main menu.

If you have not stored your last setup, the system asks you whether you want to store the last setting.

Switching the Tester Off

To switch off the Agilent 93000 SOC Series test system:

1 Press the Standby button on the front panel of the support rack.

Figure 14 Standby Button

2 For maintenance purposes only:
Put the line switch at the rear of the support rack into the OFF position.

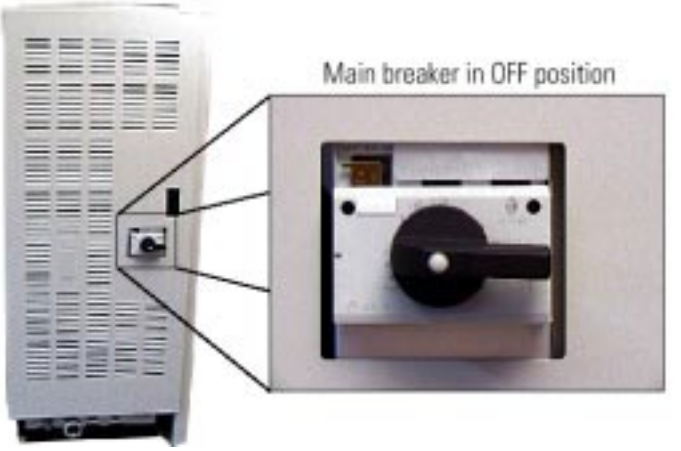


Figure 15 Line Switch in OFF position

Emergency Off

In case of emergency:

Press the red Emergency OFF button on the support rack.

This will shut down the test system and the cooling unit. The unswitched power outlets and the auxiliary power supply are still connected to mains.

3

Hardware Components

This chapter provides you with information on:

Tester Electronics

The complete tester electronics for up to 512 DUT pins (512 pins testhead) or up to 1024 pins (1024 pins testhead) resides in the testhead of the SOC Series test system.

The testhead is divided into **cardcages**. A 512 pins testhead consists of four **128 pins modules**, a 1024 pins testhead consists of eight 128 pins modules. The cardcage of each module can be equipped with channel electronics, power supply, and control boards for up to 128 DUT pins.

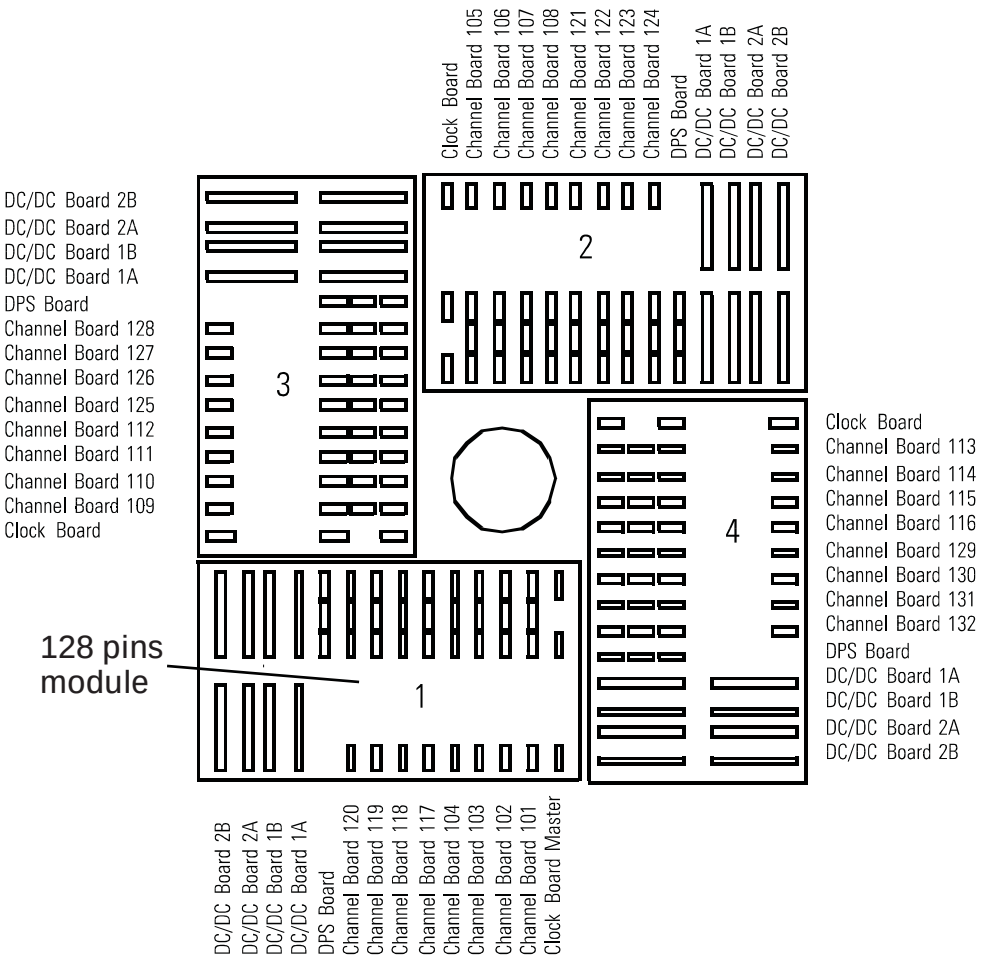


Figure 16 Tester Electronics Inside a 512 Pins Testhead

Components Inside a 128 Pins Module

Device Power Supply

The device power supplies (DPS) reside inside the testhead, which results in short cable connections and therefore low inductance. This is especially important for devices with high power consumption and high data rates.

One **DPS Board** can reside inside a 128 pins module. A DPS board contains 4 DPS channels.

A power supply channel is connected to the DUT's power supply pin (Vcc, see figure below). For multi-site testing you connect the different power supply channels to the power supply pins of the different sites.

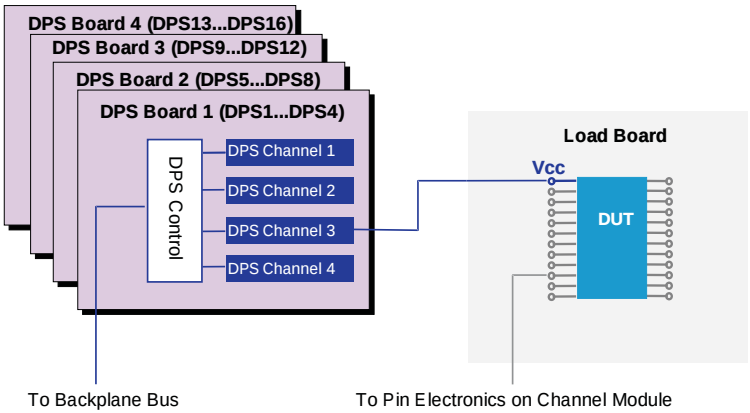


Figure 17 DPS Connection

For detailed information, refer to Chapter 6 *"Device PowerSupply"* on page 135.

Channel Boards

4 resp. 8 channels are grouped on one channel module. Each testhead slot holds a board with 4 of these channel modules, which results in 16 channels per slot or up to 512 channels in the 32 slots testhead and 1024 channels in the 64 slot testhead (if no analog function is considered)

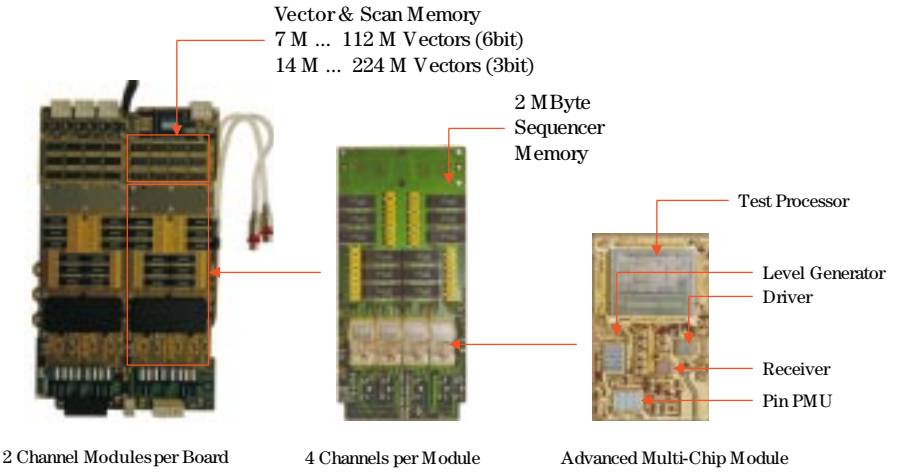


Figure 18 Channel Boards

The channel borad provides basic functions for digitial test:

- Generating digital signal to DUT
- Receiving digital signal from DUT and comparing it with expect data

And it also provides the capture function for mixed-signal test.

The figure below depicts the pin electronics on a channel board.

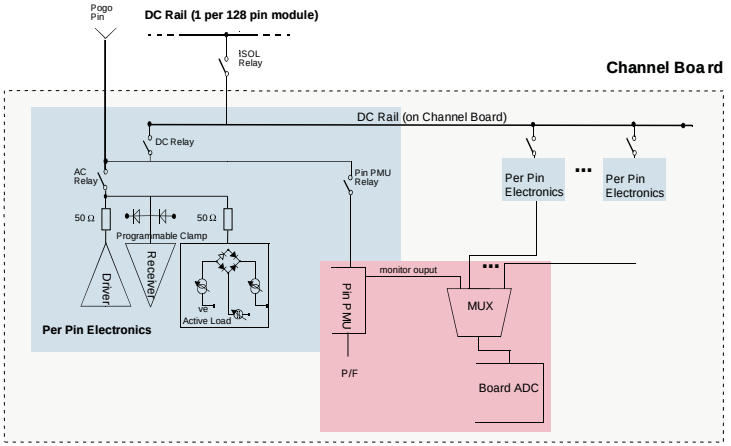


Figure 19 Channel Board Electronics

DC / DC Boards

Each 128 pins module is equipped with two DC/DC boards. The DC/DC boards generate the voltages required for all testhead resident components. They receive power supply from the AC/DC converters located in the support rack. By this, interference with the AC power is avoided completely.

Clock Board

The Clock Board provides the following resources shared by the digital channels of a 128 pins module:

The **Master Clock Generator** generates the system's master clock. The master clock is the timing reference for all timings. The master clock pulse is generated by the clock board that has been configured as master (usually the clock board of the 128 pins module 1). The master clock signal is distributed to all 128 pins modules as the timing reference of the system.

The voltages generated by the **Reference Voltage Generator** are used for DC calibration.

The **High-Precision PMU** is used for high-precision DC measurements (refer to *"High-Precision PMU"* on page 47).

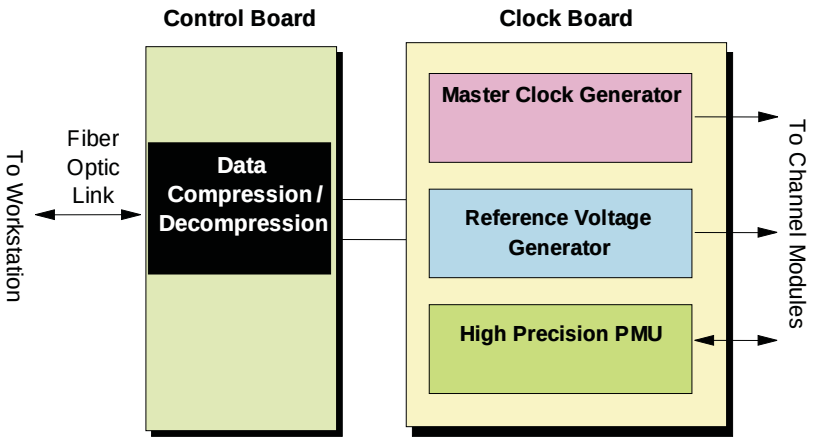


Figure 20 Clock Board

The clock board is connected to the Control Board, which provides a data/decompression circuit for vector data and makes the fiber optic connection to the workstation.

For technical details and descriptions of all components and their modes of operation, refer to the *SOC Series Service Guide*.

Analog Modules

For precision mixed-signal testing, Agilent 93000 can have the following analog modules.

- High resolution AWG (1 MSample/s 18-bit AWG)
- High speed AWG (128 MSample/s 12-bit AWG)
- Ultra high speed AWG (2.6 GSample/s 8-bit AWG)
- High resolution digitizer (2 MSample/s 16-bit digitizer)
- High speed digitizer (41 MSample/s 12-bit digitizer)
- Dual high speed sampler (1GHz 12-bit sampler)
- High performance TIA (Time Interval Analyzer)
- General purpose TIA (Time Interval Analyzer)

For the ultra high speed AWG, high performance TIA and general purpose TIA, the instruments as the main body are installed in the analog support rack and the front-end modules are installed in the testhead.

Parametric Measurement Units

The SOC Series is equipped with two types of Parametric Measurement Units (PMUs):

- Pin PMU, associated with a board ADC per 16 pins
- High-Precision PMU per 128 pins

For additional information on the PMUs, refer to the *Standard Test Function Reference*.

Pin PMU

Each digital channel provides an independent unit for DC tests—the Pin PMU.

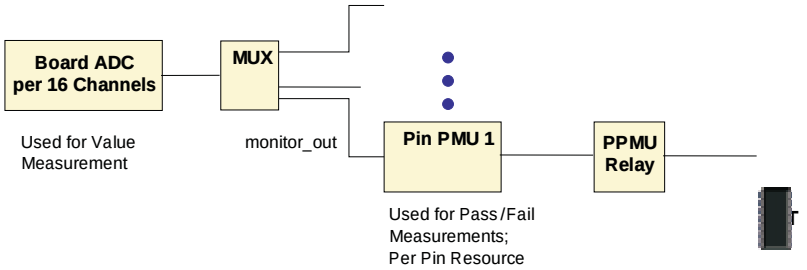


Figure 21 Pin PMU and Board ADC

The Pin PMU returns pass/fail signals to the test processor. Two compare voltage levels received from the level generator are used as thresholds.

One measurement PMU is available on each channel board comprising 16 channels.

The analog monitor output of the Pin PMU is linked to the Board ADC via a multiplexer. The Board ADC converts the analog values it receives from the Pin PMU to digital values.

The figure below shows the settling time of the parallel Pin PMU measurements and the subsequent conversion times needed for the multiplexed analog value conversions performed by the Board ADC.

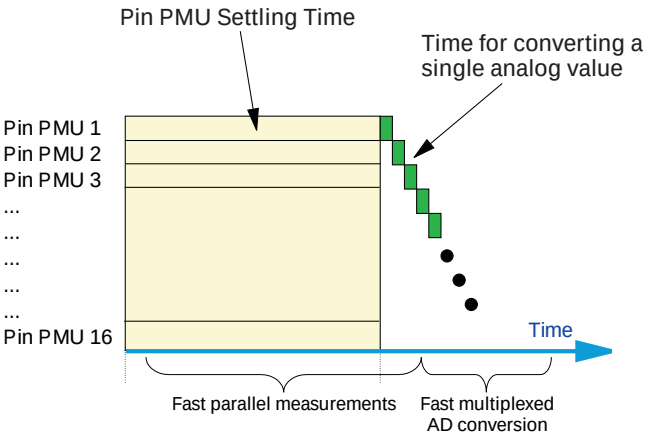


Figure 22 Multiplexed AD Conversion of Parallel Pin PMU Measurements

Settling of signals costs time. However, the Pin PMU signals can settle in parallel (parallel value measurement) saving a lot of settling time. Next, the measurement PMU performs value measurements in serial.

High-Precision PMU

For high-precision value measurements, the SOC Series provides one High-Precision PMU (HPPMU) per 128 pins module.

Voltages can be forced and currents measured (voltage force mode), or currents can be forced and voltages measured (current force mode). The High Precision PMU can be connected to any digital channel of the 128 pins module.

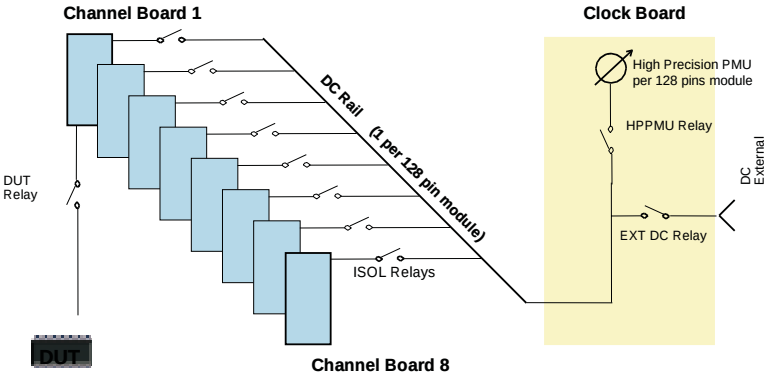


Figure 23 Connecting the High-Precision PMU to a Channel Board

You can connect the High-Precision PMUs with the channels as shown in the tables below (for the three different DUT interfaces available with the SOC Series.

HPPMU #	Channel #s
11	10101–10416, 11701–12016
12	10901–11216, 12501–12816
21	10501–10816, 12101–12416
22	11301–11616, 12901–13216

Table 1 HPPMU Connections, Agilent 83000 Style DUT I/F

HPPMU #	Channel #s
11	11701–12416
12	10101–10816
21	10901–11616
22	22501–23216

Table 2 HPPMU Connections, SOC 512 DUT I/F

HPPMU #	Channel #s
11	12501–13216
12	11701–12416
21	22501–23216
22	21701–22416
31	10101–10816
32	20101–20816
41	20901–21616
42	10901–11616

Table 3 HPPMU Connections, SOC 1024 DUT I/F

Master Clock System

The master clock is the timing reference for all timings, and the heart of the test system. The tester hardware such as the digital channel boards and analog modules use the master clock for operating the hardware.

In the world of mixed signal testing, two different master clocks are often needed to make use of the best performance of arbitrary waveform generators and waveform digitizers (including the sampler) involved in testing the device. This is especially important in performing coherent measurements as shown in the following figure.

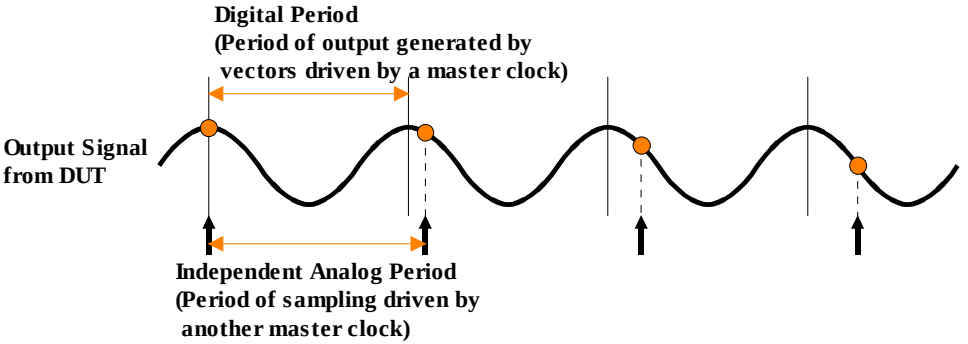


Figure 24 Coherent Sampling

Two Clock Domains

The SOC series can have two independent domains of the master clock sources. One is the "**digital clock domain**". The master clock of the digital clock domain is used for digital channel boards mainly, and it can be also used for the analog modules.

The other is the "**analog clock domain**". The master clock of the analog clock domain is used for analog modules only.

In each clock domain, you can select a master clock source from the internal master clock generator on the clock board or AMC (Alternate Master Clock generator) described in the next paragraph.

Alternate Master Clock

The **AMC (Alternate Master Clock generator)** is an optional signal generator used as a master clock generator. It is installed in the support rack and is connected to the external clock input of the clock boards in the testhead.

The AMC has better performance for the following characteristics:

- Phase Noise
- Spurious
- Intermodulation

Therefore, the AMC generates a master clock with lower jitter, and enables the tester hardware to operate with more accurate timing for high speed applications using the Dual High Speed Sampler (undersampling) and High Speed AWG.

If you perform precision mixed-signal testing such as these, AMCs should be used for both the digital and analog clock domains. However, note that the AMC's frequency switching speed is slower than for the internal master clock generator.

The setting range and resolution of the AMC are as follows:

Range:	2 - 5 ns (200 MHz - 500 MHz)
Max. Resolution:	Approx. 10 digits (0.01 Hz)

For more technical information of the AMC, contact an Agilent Technologies sales and service office.

For the master clock generator on the clock board,

Range:	2 - 5 ns (200 MHz - 500 MHz)
Max. Resolution:	15 digits (approx. 1 μHz)

Note that there are some restrictions about maximum resolution that can be programmed on the software for digital channels using fixed timing. You can avoid them if timing equations are used.

Master Clock Distribution

In the case of a single master clock, the master clock of the digital clock domain is used for both digital channel boards and analog modules. The master clock generated from the clock board in cardcage #1 on the 512-pin testhead or #5 on the 1024-pin testhead or the digital clock domain's AMC is distributed around the ring of all boards in other cardcages. Hence, both digital channel boards and analog modules use the master clock of the digital clock domain.

In the cage of two master clocks, the master clock of the digital clock domain is used for all the digital channel boards. The master clock generated from the clock board in cardcage #1 on the 512-pin testhead or #5 on the 1024-pin testhead or the digital clock domain's AMC is distributed around the ring of all digital boards and some analog modules in other cardcages.

For each analog module, you can select the desired clock domain from the digital or analog clock domains. If you select the master clock of the digital clock domain for an analog module, the analog module uses the same master clock used for the digital channel boards. That is, it uses one master clock for both digital channel boards and analog modules.
If you select the master clock of the analog clock domain, the analog module uses the master clock generated from the clock board in it's own cardcage or the analog clock domain's AMC. This means it uses a different master clock from the master clock of the digital clock domain.

All master clock sources are phase-locked on the distributed 10 MHz reference from one of the following:

- Digital clock domain's AMC
- Analog clock domain's AMC
  (if no digital clock domain's AMC is configured)
- Clock board in cardcage #1 on the 512-pin testhead or #5 on the 1024-pin testhead (if no AMC is configured)

The following figures show the master clock distribution on the 512-pin and 1024-pin testheads. The hardware configuration and connections are shown in a simplified for easy understanding.

The master clock generators on the clock boards in cardcages #2 and #4 on the 512-pin testhead or cardcages #2, #4, #6 and #8 on the 1024-pin testhead are used with the same setting condition for analog modules, if the master clock generated from the clock board is selected.
The master clock from the analog clock domain's AMC is split by the power splitter once, then the split clocks are directly sent to the clock boards in the cardcages where the analog modules are installed.

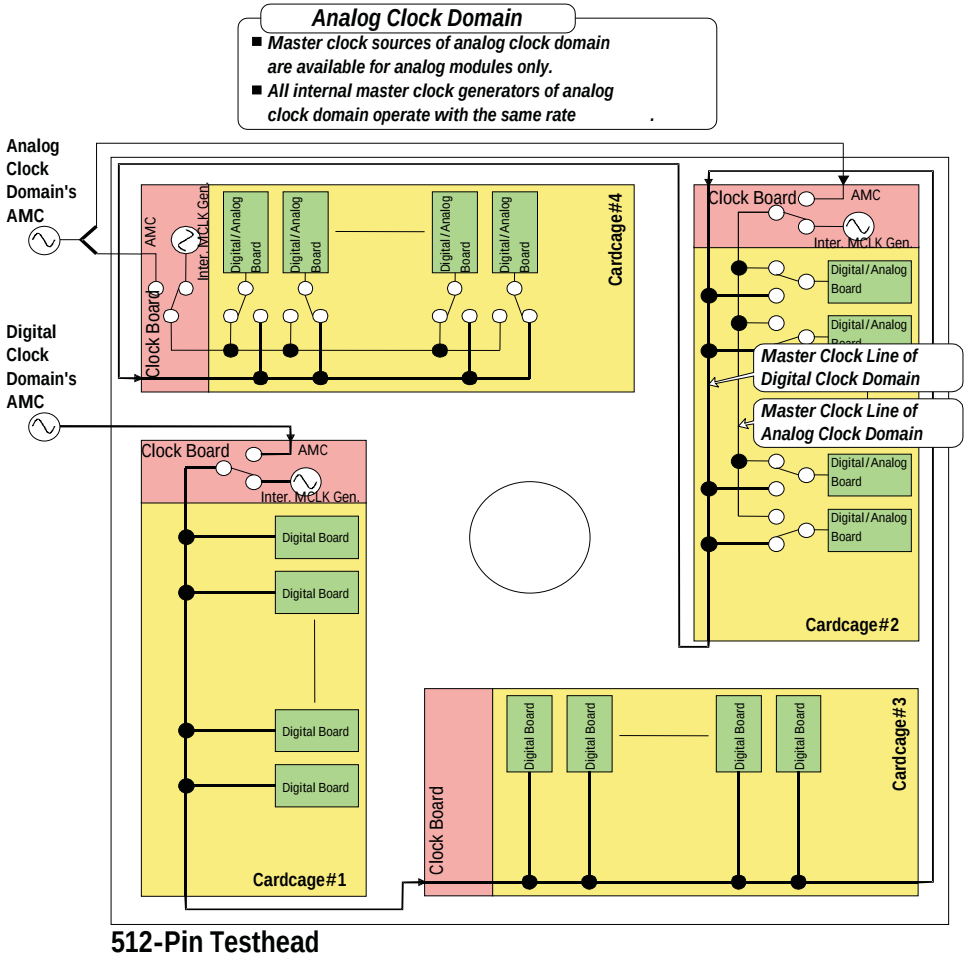


Figure 25 Master Clock Distribution on 512-Pin Testhead

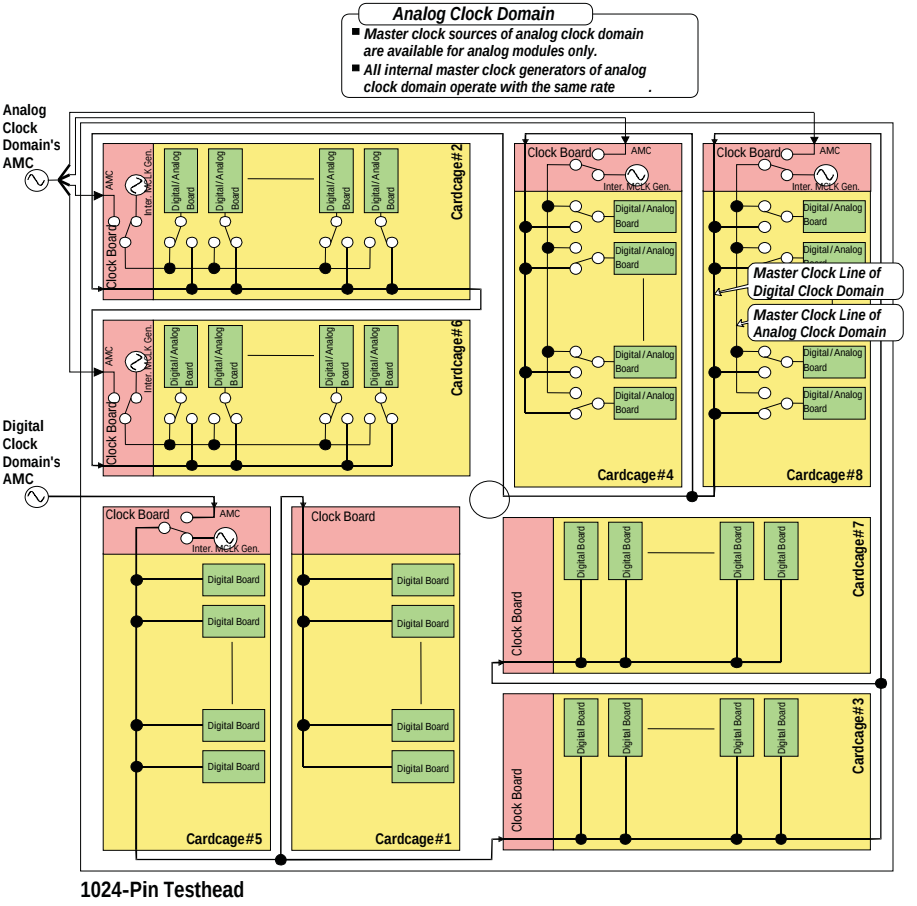


Figure 26 Master Clock Distribution on 1024-Pin Testhead

Available Master Clock Sources

Available master clock sources for tester hardware are as follows:

All digital channel boards:

- Digital clock domain
  - Internal master clock generator in cardcage #1 on the 512-pin testhead or #5 on the 1024-pin testhead
  - Digital clock domain's AMC

All analog modules:

- Digital clock domain
  - Same master clock source used for the digital channel boards (one master clock used)
- Analog clock domain
  - Internal master clock generator in the cardcage where the analog module is installed
  - Analog clock domain's AMC

4

Test Head Filling and DUT Board Considerations

This chapter covers the DUT board structure and how to equip the test head with digital boards and analog modules.

The chapter is divided into the following four sections:

- *"Overview of Test Heads"* on page 59.
- *"DUT Board Mechanical Considerations"* on page 61 concerning the packaged parts DUT boards.
- *"Test System Configuration"* on page 70 from the view of the packaged parts DUT boards. But note that most of the information given in this section is also valid for the wafer prober DUT boards.
- *"Wafer Prober DUT Board and Probe Card"* on page 104.

You will be served with all information necessary to:

- know about filling options and filling of your test head with analog modules.
- get an overview of the DUT board contacting schemes.
- read the nomenclature of the DUT board drawings for future DUT board designs or changes.

Web Address of the DUT Board Design Guide

Together with the Drawings and the Agilent 93000 DUT Board Design Guide (www.ate.agilent.com/ste/members/member_index.shtml) you should then be able to design your customized DUT board.

In case you want it to **be** designed or/and manufactured for you contact an Agilent Representative for assistance.

Overview of Test Heads

The Agilent 93000 SOC Series comes with a 512 pin and a 1024 pin test head.

The two versions of the tester together with a sketch of their test heads are shown in *Figure 27*.

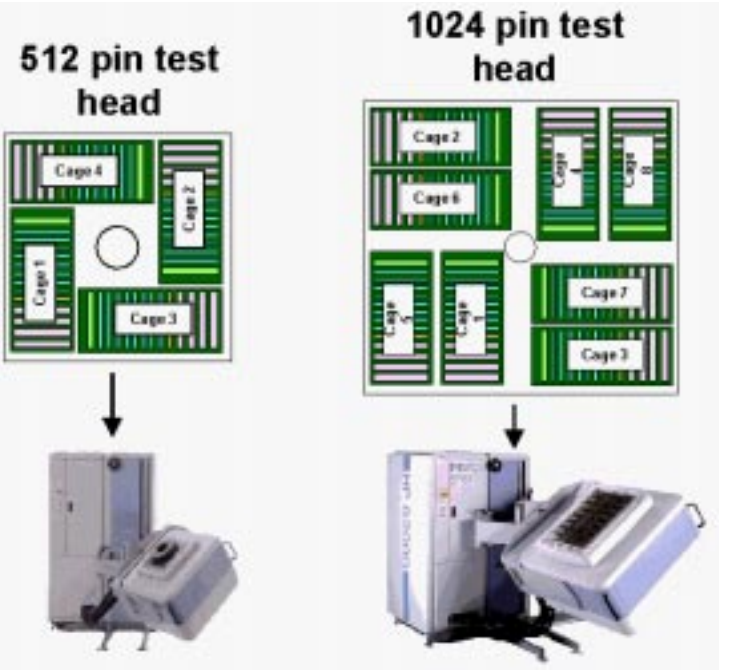


Figure 27 Card Cage Positions within Test Head (Topview from DUT Board Side) above their Corresponding SOC Series Testers.

As you can see in *Figure 27*, the 512 pin testhead supports 4 card cages while the 1024 pin testhead supports 8 card cages. Each card cage can contain 8 digital boards or 8 analog modules respectively. A single board has 16 pins making 128 pins per cage. Therefore, the four caged test head contains 512 pins and the 8 caged test head 1024 pins.

Structure of Card Cages

Figure 28 illustrates the structure of a card cage.

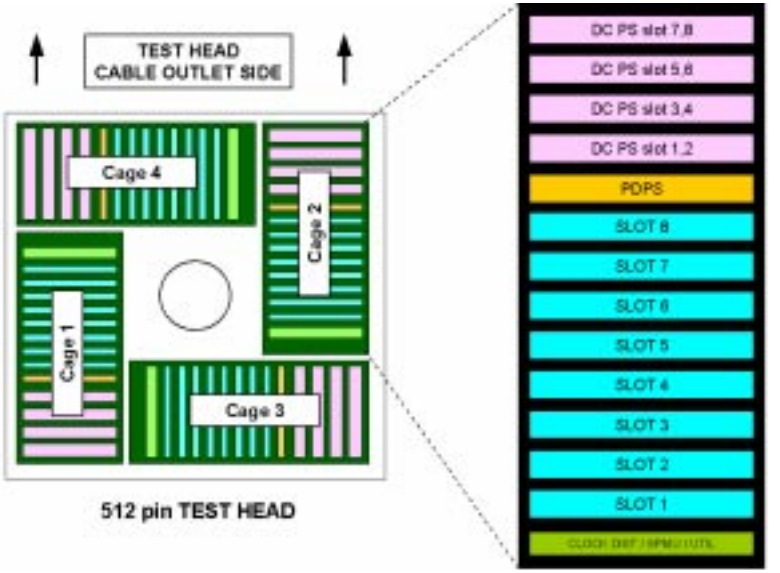


Figure 28 Input of a card cage

A card cage has the following content:

- **CLOCK DIST** refers to the clock signal distribution in each single cage run by a clock board receiving their clock signals from a distributing master clock situated in only one of the cages.
- In **two to four** of the card cages there is a high precision High Precision Parametric Measurement Unit **(HPMU**).
- **UTIL** referes to utility lines inherent in the card cages.
- The 8 so called **SLOT**s contain the previously mentioned digital boards or analog modules.
- The device power supply is run by the **PDPS.**
- The **DC PS** slots contain DC DC converters for two of the **SLOT**s each.

DUT Board Mechanical Considerations

This section gives you an overview of the mechanical structure of the SOC series **packaged parts** DUT boards.

NOTE: Starting from here up to the end of this chapter, *DUT board* is used synonymously to *packaged parts DUT board*.

Figure 29 on page 61illustrates the placing of the packaged parts DUT board above the test head.

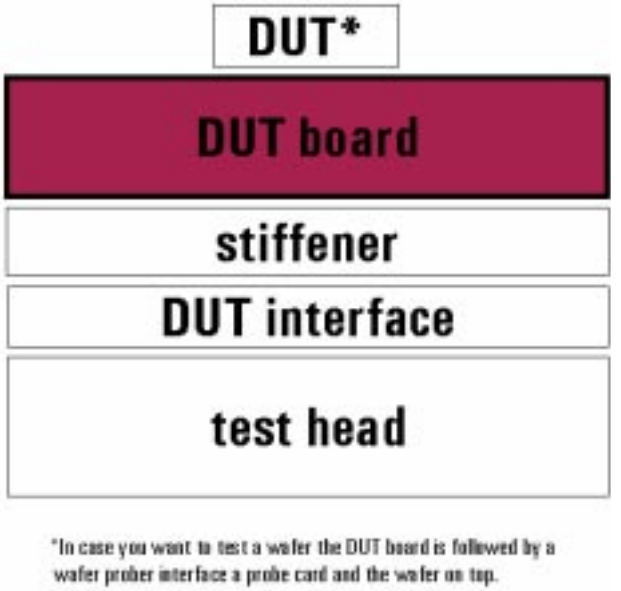


Figure 29 Position of DUT board above the Test Head.

Instead of

- a **packaged parts DUT board** ,

where the devices under test are placed directly on the DUT board,

- a **wafer prober DUT board**

can be placed on top of the DUT interface followed by several further components as illustrated in *Figure 45* on page 104.

For an overview of **wafer prober** DUT boards see *"Wafer Prober DUT Board and Probe Card"* on page 104.

Overview of DUT Board Options

With the 512 pin and the 1024 pin version of the tester you have the following DUT board options:

- On the **1024 pin test head** you will normally use a 1024 pin SOC Series DUT board but you can use a 512 pin SOC Series DUT board aswell.
- On the **512 pin test head** you will normally use a 512 pin SOC Series DUT board. You can also reuse an Agilent 83000 F330 DUT board with this test head but **only** in combination with an F330-Style DUT interface.
- For engineering samples Agilent supports **256 pin SOC Series DUT board**s for both the 512 pin and the 1024 pin test head. See *"Possible 256 pin DUT boards for either the 512 pin test head or the 1024 pin test head"* on page 66 for detail on which sections of the 1024 pin DUT board can be used as 256 pin DUT boards. **NOTE** that you **can't** use the 256 pin DUT board for production since it is impossible to place the handler that has to be located in the center of the test heads on any 256 pin DUT board.

Figure 30 shows which of the three optional DUT boards fits which version of the SOC series tester.

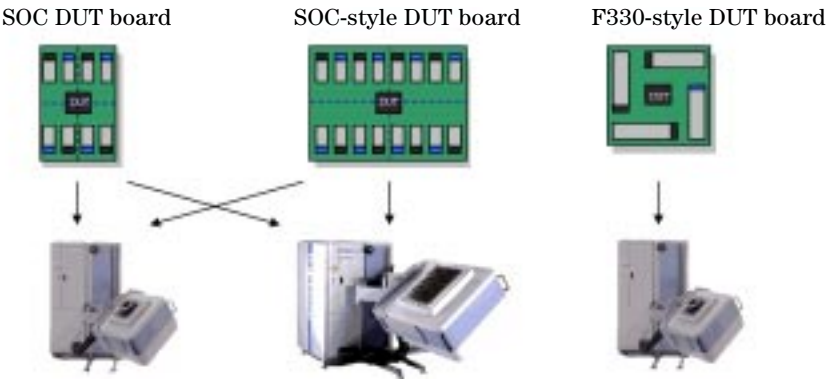


Figure 30 DUT board options depending on test head size

In *Figure 30* the 1024 pin version of the SOC series tester is situated in the center and a 512 pin version is situated to either side of the 1024 pin tester. The 1024 pin SOC series DUT board in the center and the 512 pin SOC series DUT board on the left have so called **halfgroup**s (lightly shaded (yellow) boxes) containing 64 pins each. The half-groups are situated in two parallel rows on each side of the DUT.

On the right of *Figure 30* you can see a F330 style DUT board. The four larger light boxes represent four so called **group**s. Each group contains 128 signal lines each.

The parallel alignment of the half groups on the SOC-style DUT boards provides more space permitting you to test more and larger DUTs at the same time.

NOTE that you can use either of the two SOC series DUT boards flexibly on either of the two testheads.

Allocation of Card Cages

Each card cage has a corresponding group on the DUT board. You can find the description for the 512 pin DUT board in *"Allocation on the 512 pin DUT Board"* on page 64 and for the 1024 pin DUT board in *"Allocation on the 1024 pin DUT Board"* on page 65.

Allocation on the 512 pin DUT Board

See also drawing D-E6980-96540-1S14D

In *Figure 31*you can see which of the card cages of the 512 pin test head match which of the groups on the 512 pin DUT board. **NOTE** that the numbers of the groups have nothing in common with the numbers of the card cages.

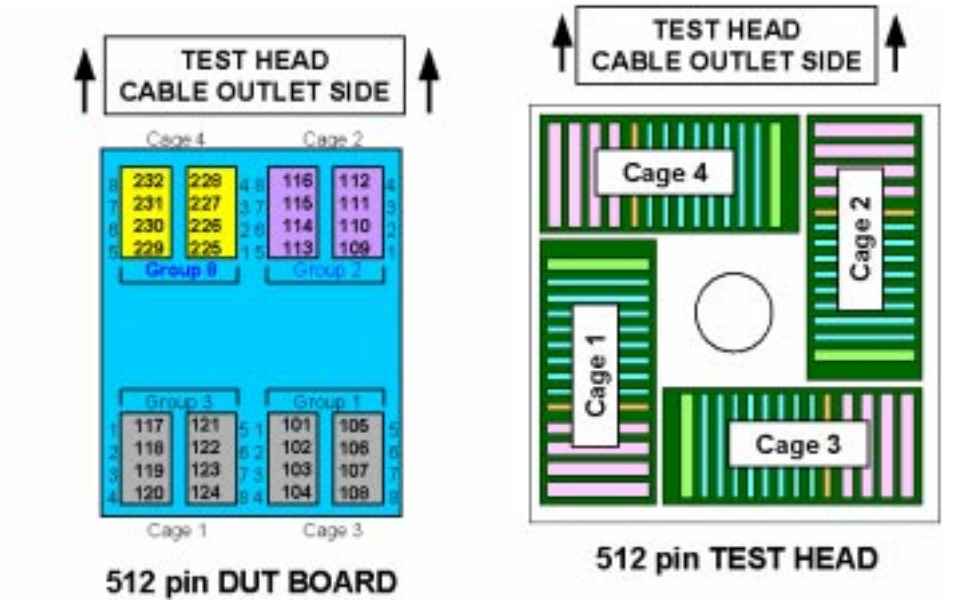


Figure 31 1. Allocation of the 512 pin DUT board's groups to the card cages of the 512 pin test head. 2. Numbering of pairs of pad blocks.

On the left side of *Figure 31*, for example, you can see that group 8 matches with card cage 2.As previously mentioned, the smaller light boxes on the DUT board illustration are called half groups. Each half group contains four pairs of so called **pad blocks**. A pad block is the landing area of a pogo pin block on the DUT board's pads. The numbers in the illustrated half groups are each assigned to one pair of pad blocks. For the description of a pair of pad blocks see *"Pad Blocks"* on page 67. **NOTE:** The correlation of the pairs of pad blocks to the affiliated slots in the card cages is shown by the slot numbers next to the half groups.

Allocation on the 1024 pin DUT Board

See also drawing D-E6980-96550-1S14D

In *Figure 32* you can see which of the card cages of the 1024 pin test head match which of the groups on the 1024 pin DUT board. **NOTE** that the numbers of the groups have nothing in common with the numbers of the card cages.

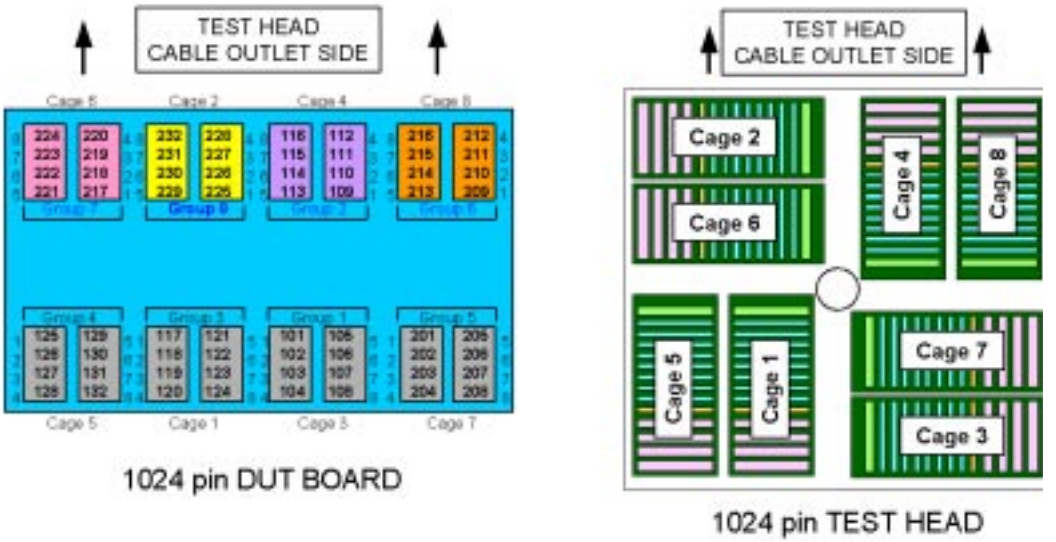


Figure 32 1. Allocation of the 1024 pin DUT board's groups to the card cages of the 1024 pin test head. 2. Numbering of pairs of pad blocks.

On the left side of *Figure 32*, for example, you can see that group 7 matches with card cage 6. As previously mentioned, the smaller light boxes on the DUT board illustration are called half groups. Each half group contains four pairs of so called **pad block**s. A pad block is the landing area of a pogo pin block on the DUT board's pads. The numbers in the illustrated half groups are each assigned to one pair of pad blocks. For a description of a pair of pad blocks see *"Pad Blocks"* on page 67. **NOTE:** Each pair of pad blocks on the DUT board corresponds to a slot inside a card cage. This is illustrated by the number of a slot next to the number of the affiliated pair of pad blocks.

Possible 256 pin DUT boards for either the 512 pin test head or the 1024 pin test head

See also drawing D-E6980-96530-1S34D

Additionally to the 1024 pin and the 512 pin DUT board you can have a 256 pin DUT board. The advantage of the 256 pin DUT board is that it is smaller and therefore cost saving.

NOTE: Normally a 256 pin DUT board is for engineering use. In case you want to use a 256 pin DUT board for production, make sure that the handler is able to reach the DUT since the DUT can't be placed in the center of the DUT interface in case of a 256 pin DUT board.

There are four possibilities of configuring a 256 pin DUT board. You can decide for one of four quarters of the 1024 pin DUT board. Each quarter contains one of the upper line groups illustrated in *Figure 32* on page 65 and the adjacent group of the bottom line.

On your 256 pin DUT board you can have either:

1. **group 8** and **group 3**.
2. **group 2** and **group 1**.
3. **group 7** and **group 4**.
4. **group 6** and **group 5**.

Your choice for one of the pairs of groups should depend on the groups' properties according to your requirements. These properties as digital dominant, analog dominant, and/or analog instrumentation are given through your customized tester configuration. See *"Test System Configuration"* on page 70 for configuration aspects.

The first two of the above listed possibilities can either be used on the 512 pin or the 1024 pin DUT interface. The third and the fourth possibilities can only be used on the 1024 pin DUT interface.

Make sure that your 256 pin DUT board possibility is located in that area of the DUT interface where the pogo pins of your pair of groups come out.

Warning: Locating the 256 pin DUT board on the pogo pin area of two different groups for which it was not designed you will have to reconfigure your pins and very likely will have to change your card cage filling which may be impossible because of your tester configuration.

Pad Blocks

See also drawings D-E6980-96540-1S14D (512 pins) and D-E6980-96550-1S14D (1024 pins)

As previously mentioned the pad blocks come in pairs of two. *Figure 33* on page 67illustrates such a pair.

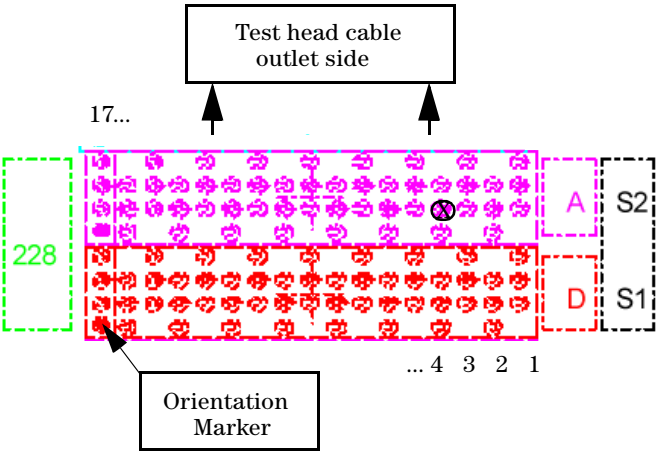


Figure 33 A Pair of Pad Blocks (No. 228)

In *Figure 33* on page 67 the two horizontal boxes are such a pair of pad blocks. The dots inside the boxes represent the pads. One pad block consists of 16 signal pads which connect to the 16 pins on a digital board or an analog module. Each of these signal pads is surrounded by three or four ground pads. This leads to three pads in a column and 8 signal pads in the two middle rows of a block. A 17th

column is currently not in use for digital measurement. You can find the number of a column below and above the pair of blocks in *Figure 33*.

Numbering of pads:

To refer to one of the signal pads on a pad block, the number of the pair of pad blocks is followed by the number of the column which contains the pad. For example: The crossed pad (column No. 4) of the upper pad block would be 22804 as this pair of blocks is pair No.228. The first integer of the number of the pair of pad blocks is either 1 or 2. The next two integer numbers go from 1 to 32 inclusive. For the numbering of the pad blocks see *Figure 31* on page 64and *Figure 32* on page 65.

See also drawing D-E6980-96540-1S34D (512 pins) and D-E6980-96550-1S34D (1024 pins)

Which pad block of the pair to use:

- If you are using a **digital board** in the corresponding slot of the pad block pair on the test head, all pogo pins of the same board **only** connect to pad blocks which are labelled **D** (for **D**igital) or synonymously **S1** (see *Figure 34*). Pad blocks labelled **S2** within groups that can exclusively contain digital boards are presently not in use.
- If you are using an **analog board** in the corresponding slot of the pad block pair within the test head, all pogo pins of the same board **only** connect to pad blocks labelled **A** (for **A**nalog) or **S2** (see *Figure 34*).

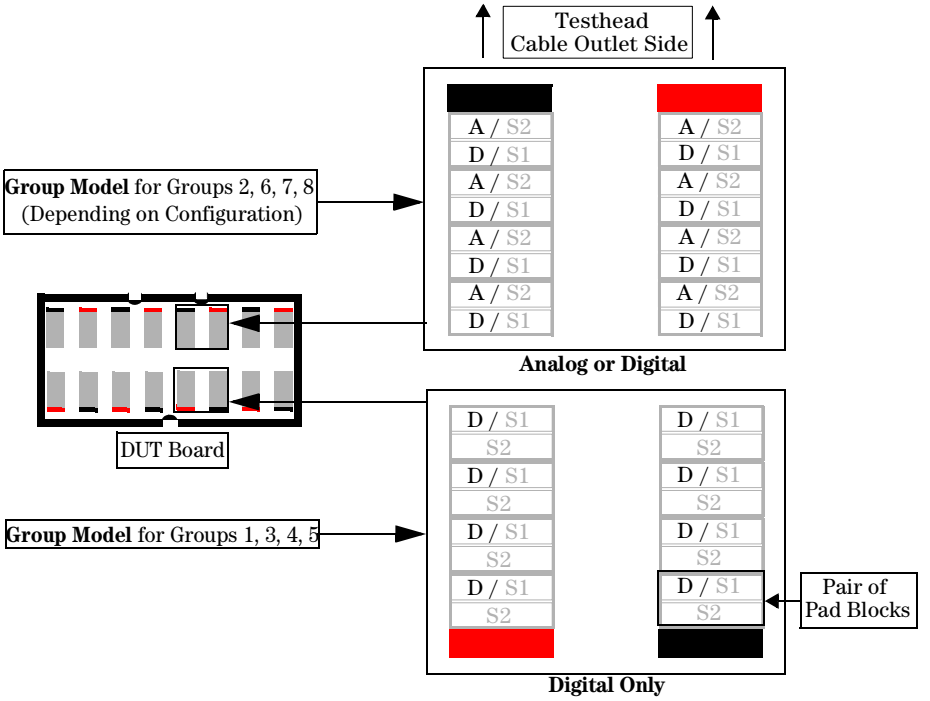


Figure 34 Position of Analog and Digital Pad Blocks within Groups

Test System Configuration

There are two types of test heads for the SOC series tester. They are the so called **digital dominant** type and the so called **analog dominant** type. The digital dominant type supports more digital pins the analog dominant one supports more analog modules. The maximum number of digital pins and analog modules in each case is shown in *Table 4* on page 70.

	Digital Dominant	Analog Dominant
512 pin test head	• Max. digital pins: **512** • Max. analog modules: **8**	• Max. digital pins: **256** • Max. analog modules: **16**
1024 pin test head	• Max. digital pins: **1024** • Max. analog modules: **24**	• Max. digital pins: **768** • Max. analog modules: **32**

Table 4 Maximum of digital pins and analog modules

Within the two types, certain groups on the DUT board will be **reserved** for digital boards as others will be **reserved** for analog modules. Some of the groups can either contain analog modules or digital boards. **Attention: Analog Module's specifications can only be guaranteed for those groups containing analog modules only.**

NOTE that referring to reserved **groups** rather than reserved **cages** describes the **test head filling** from a DUT board point of view. This is explained in *"Digital Dominant Configuration"* on page 71 and in *"Analog Dominant Configuration"* on page 74 for both the 512 pin and the 1024 pin SOC series tester.

Digital Dominant Configuration

The first part of this section deals with the 512 pin SOC series tester as the second part with the 1024 pin SOC series tester:

1. The reservation of groups of the digital dominant type of the 512 pin SOC series tester is illustrated in *Figure 35*.

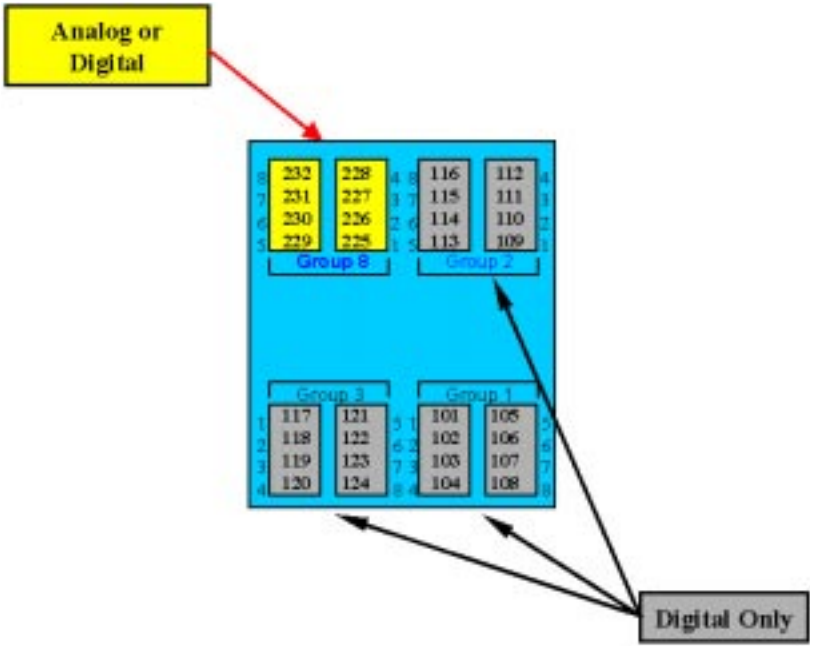


Figure 35 Group reservation of the digital dominant type 512 pin SOC series tester

As shown in *Figure 35*, the only place for analog modules is in group 8 which can optionally accomodate digital boards or analog modules. **NOTE that Analog Module's specifications can only be guaranteed if group 8 contains analog modules only.**
Groups 1-3 can only contain digital boards.

There is a filling algorithm for filling the test head with digital boards and analog modules:

- Digital Filling:
  Group 1 ---> Group 2 ---> Group 3 ---> (Group 8)
- Analog Filling:
  (Group 8) **only**

The bracket indicates that group 8 can **optionally** be used for digital or analog testing. For this reason you can find it under both list items.

This system configuration has the following maximum analog and maximum digital configuration:

- Maximum Analog:
  8 analog modules ---> **384** digital pins
- Maximum Digital:
  no analog modules ---> **512** digital pins

The **main advantage of the digital dominant configuration of the 512 pin tester compared to the analog dominant type of the 512 pin tester** is that digital is populated in the groups on the bottom line of the DUT board as well as in the upper line groups. This makes DUT board routing for digital signals much simpler.

2. The reservation of groups of the digital dominant type of the 1024 pin SOC series tester are illustrated in *Figure 36*.

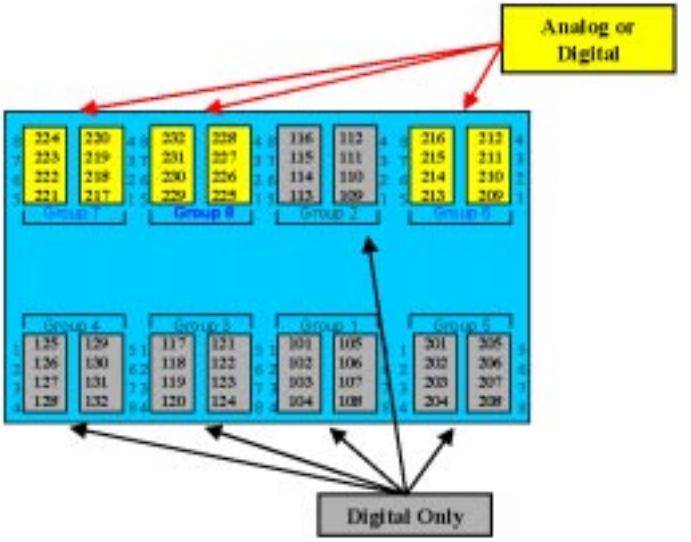


Figure 36 Group reservation of the digital dominant type 1024 pin SOC series tester

The lightly shaded (yellow) groups in *Figure 36* are the only ones that can contain analog modules. Optionally, you can have digital boards or analog modules in these three groups. **NOTE that Analog Module's specifications can only be guaranteed if these groups contain analog modules only.**

The more heavily shaded (dark grey) groups can only contain digital boards.

There is a filling algorithm for filling the test head with digital boards and analog modules:

- Digital Filling:
  Group 1 ---> Group 2 ---> Group 3 ---> Group 4 ---> Group 5 ---> (Group 7) ---> (Group 6) ---> (Group 8)
- Analog Filling:
  (Group 8) ---> (Group 6) ---> (Group 7)

The bracket indicate that groups 6, 7 and 8 can **optionally** be used for digital or analog testing. For this reason you can find those groups under both list items.

This system configuration has a maximum analog and a maximum digital configuration:

- Maximum Analog:
  24 analog modules ---> **640** digital pins
- Maximum Digital:
  no analog modules ---> **1024** digital pins

Analog Dominant Configuration

The first part of this section deals with the 512 pin SOC series tester as the second part deals with the 1024 pin SOC series tester:

1. The reservation of groups of the analog dominant type of the 512 pin SOC series tester is illustrated in *Figure 37*.

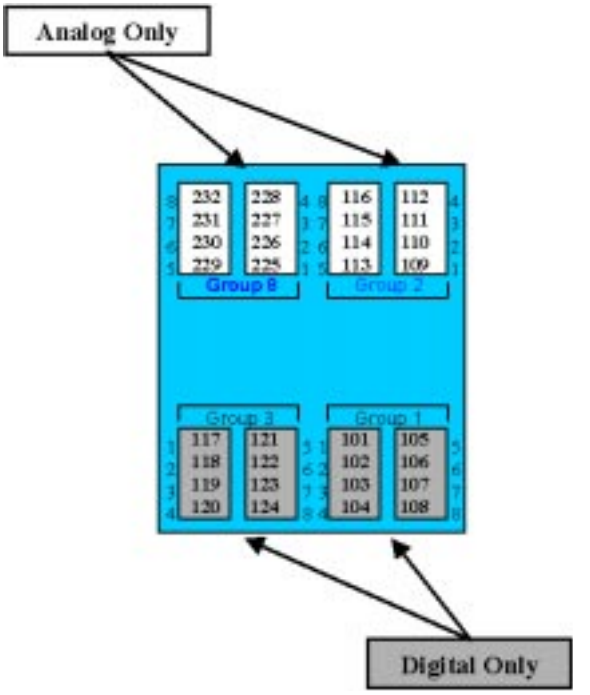


Figure 37 Group reservation of the analog dominant type 512 pin SOC series tester

The unshaded (white) groups in *Figure 37* can contain analog modules only. The shaded (dark grey) groups can only contain digital boards.

There is a filling algorithm for filling the test head with digital boards and analog modules:

- Digital Filling:
  Group 1 ---> Group 3

- Analog Filling:
  Group 8 ---> Group 2

This system configuration has a maximum analog and a maximum digital configuration:

- Maximum Analog:
  16 analog modules ---> **256** digital pins
- Maximum Digital:
  The same as above.

The **main advantage of the analog dominant configuration of the 512 pin SOC series tester** is that up to 16 analog modules can be supported.

2. The reservation of groups of the analog dominant type of the 1024 pin SOC series tester is illustrated in *Figure 38*.

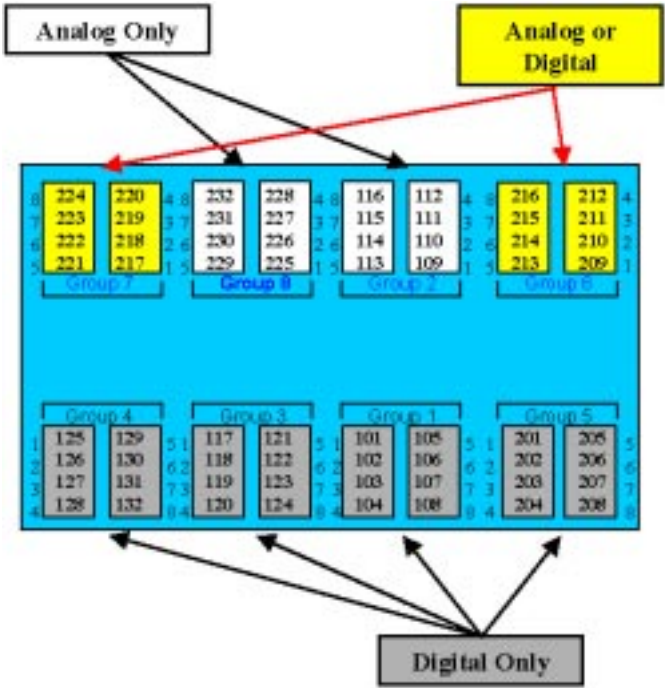


Figure 38 Group reservation of the analog dominant type 1024 pin SOC series tester

As shown in *Figure 38*, the upper light groups on the DUT board is for analog modules -- the unshaded (white) groups for analog modules only the light shaded (yellow) groups optionally for analog modules or digital instead. **NOTE that Analog Module's specifications can only be guaranteed in case that the optional groups 6 and 7 contain analog modules only.**

The heavily shaded (dark grey) groups in the lower row are reserved for digital boards only.

There is a filling algorithm for filling the test head is to be filled with digital boards and analog modules:

- Digital Filling:
  Group 1 ---> Group 3 ---> Group 4 ---> Group 5
  ---> (Group 7) ---> (Group 6)
- Analog Filling:
  Group 8 ---> Group 2 ---> (Group 6) ---> (Group 7)

The brackets indicate those groups that can optionally be used for digital or analog testing. For this reason you can find those groups listed under both list items.

This system configuration has a maximum analog and a maximum digital configuration:

- Maximum Analog:
  32 analog modules ---> **512** digital pins
- Maximum Digital:
  16 analog modules ---> **768** digital pins

Overview of Filling

The card cage filling options are listed in *Figure 38*.

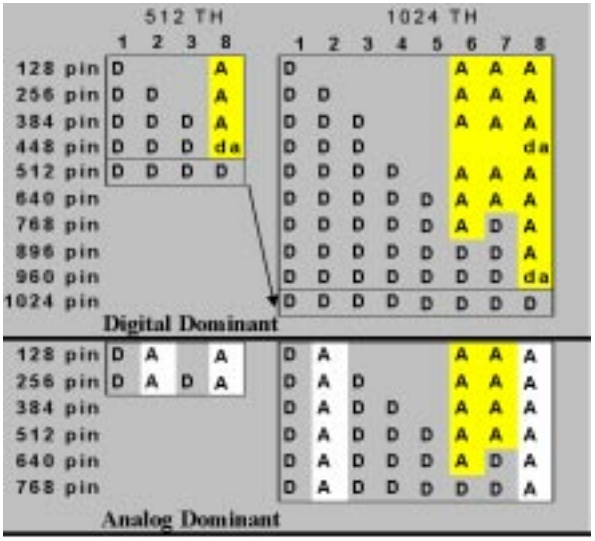


Figure 39 Card Cage Filling Options from DUT board "view"

In the top two squares in *Figure 39*, the filling options within the **digital dominant** type for the 512 pin and the 1024 pin SOC series tester are listed. In the bottom squares you can find the **analog dominant** filling options. The filling is of the following four kinds: **A**, **D**, **a** and **d**.

- **A** stands for analog filling in an entire group.
- **D** stands for digital filling in an entire group.
- **a** stands for analog filling (**digitizers only**) in a half group only.
- **d** stands for digital filling in a half group only.

In extreme conditions, where very high pin counts (448 pins for 512 pin test head or 960 pins for 1024 pin test head) are required a **d-a** split of analog-digital within a

single group will be supported. **NOTE** that only digitizers are possible in such an analog half group and that **Analog Module's specifications can not be guaranteed.**

The numbers on top of the squares in *Figure 39* are those of the groups that are filled in that column.
The numbers on the left hand side of the boxes indicate the maximum number of digital pins you can obtain for the filling mentioned in the same row.
The colour coding is the same as in *Figure 38* for the group reservations: white for analog only, lightly shaded (yellow) for optionally digital or analog and heavily shaded (dark grey) for digital only.
The first four rows of the 1024 pin test head digital dominant filling contains the same number of digital pins as the corresponding four rows of the 512 pin test head. Thus if you use the 1024 pin DUT board on the 512 pin test head your maximum number of digital pins will stay the same. This is the same for the first two rows of the analog dominante case.
The last and seperated row of the digital dominant 1024 pin tester filling option is the only one differing: For that row the maximum number of digital pins corresponds to that one of the last row of the 512 pin digital dominant tester as indicated by the arrow.

Digital Fill Order

The digital input-output channels are filled according to increasing pad numbers starting from the lowest pad number of group 1 which is 10101. (For the numbering of groups and pads see *"Pad Blocks"* on page 67.) A group (two adjacent halfgroups of four pairs of pad blocks each) is to be completely filled with up to 128 digital channels, before you start filling another group. See *"Digital Dominant Configuration"* on page 71 or *"Analog Dominant Configuration"* on page 74 to know which group is to be filled next and continue filling with increasing pad numbers.

List of Analog Instruments

In *Table 5*, the analog instruments are listed according to **source** and **measurement** depending on their functionality.

- **Source** analog instruments generate the analog INPUT signal which goes into the DUT. Such analog signal generators are so called **AWG**s (**A**rbitrary **W**afeform **G**enerators).
- **Measurement** analog instruments measure the analog DUT OUTPUTs. These measuring instruments such as **Digitizer**s, **Sampler**s and **TIA**s (**T**ime **I**nterval **A**nalyser) sample or time analyse the analog output.

SOURCE
LF: 1 MHz/ 18-bit High Resolution
VHF: 128 MHz/ 12-bit High Speed AWG
UHF: 2.6 GHz/ 8-bit Ultra High Speed AWG
MEASURE
LF: 2 MHz/ 16-bit High Resolution Digitizer
VHF: 40 MHz/ 16-bit High Resolution Digitizer
SAMP: 1 GHz/ 12-bit Dual High Speed Sampler
TIA: High Performance TIA General Purpose TIA (under investigation)

Table 5 List of Analog Instruments

Analog Fill Order

The order of analog filling depends on the test head configuration. Therefore, the fill order for the digital dominant configuration is described in part one of this section while you can find that one for the analog dominant configuration in part two.

1. The fill order of the analog instruments (see *Table 5*) is illustrated in *Figure 40* for the **digital dominant** configuration.

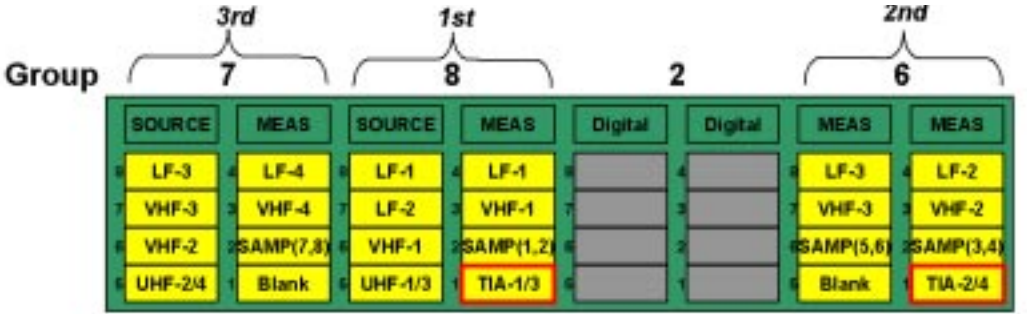


Figure 40 Fill Order of Analog Instruments within the Digital Dominant Configuration

In *Figure 40* the six lightly shaded (yellow) boxes are the half groups of those three groups which can support analog instrument within the 1024 pin digital dominant configuration. Thus, for this configuration the analog instruments can only be placed in those card cages corresponding to groups 6, 7 and 8. In the 512 pin digital dominant configuration the analog instruments can only be placed in the card cage slots corresponding to group 8.

The analog time analysing or measuring instruments are placed in the half groups titled **MEAS**. The analog signal generators are placed in the half groups titled **SOURCE**. Depending on the half group the abbreviations of the analog instruments correspond either to **source** or **measurement** in the table in *Table 5*. The numbers next to an abbreviation assign the count number of an instrument type. These count numbers increase with increasing filling of the cages.

The fill order of the cages is marked above the brackets at the top of the group scheme in *Figure 40*.

NOTE: This is the fill order to follow. The fill order mentioned in the drawing E6980-96550-1S3 is INVALID. The slot number of the slots, where an analog module has to go within the cage, is mentioned to the left of the half groups.

A **TIA** test head card always comes with a GP TIA and either with a second GP TIA or, optionally, with a HP-TIA. The first card containing a GP TIA is placed in slot 1 of group 8 and the second one is placed in the first slot of group 6. In each of the two slots, you can chose one of the two optional TIAs on top (marked “slot b” in the table in *Table 6*). This way you can obtain a maximum number (MAX) of 4 GP TIAs. Otherwise, you can have up to 2 HP TIAs but in this case only 2 GP TIAs.

In the case of the sampling instruments, there are two samplers in a slot as the **sampler**sare **dual** and thus two count numbers each are assigned in *Figure 40*. Therefore, the maximum number of single samplers is additionally mentioned in brackets in the table in *Table 6*.

NOTE that group 6 supports **MEAS**urement only to increase the number of digitizers without compromising the number of digital channels. The Agilent source channels (except UHFAWG) have buffered outputs so that fan out to multisite is made simple. Therefore, more digitizers are desireable for multisite and allowing **MEAS**urement to be supported in an entire group makes this possible.

The **blank** slots in *Figure 40* are kept for future enhancements.

Source	1st	2nd	3rd	4th	Max
LF-AWG	group 8 slot 8	group 8 slot 7	group 7 slot 8		3
VHF-AWG	group 8 slot 6	group 7 slot 6	group 7 slot 7		3
UHF-AWG	group 8 slot 5a	group 8 slot 5b	group 7 slot 5a	group 7 slot 5b	2
Measure					
LF-DGTZ	group 8 slot 4	group 6 slot 4	group 6 slot 8	group 7 slot 4	4
VHF-DGTZ	group 8 slot 3	group 6 slot 3	group 6 slot 7	group 7 slot 3	4
SAMP (2)	group 8 slot 2	group 6 slot 2	group 6 slot 6	group 7 slot 2	4(8)
GP-TIA	group 8 slot 1a	group 6 slot 1a	group 8 slot 1b	group 6 slot 1b	2(4)
HP-TIA	group 8 slot 1b	group 6 slot 1b			2(0)

Table 6 Analog Instruments, Count and Filling for the Digital Dominant Configuration

The numbers above the columns of the table in *Table 6* referre to the counting numbers of the analog instruments.

2. The fill order of the analog instruments (see *Table 5*) is illustrated in *Figure 41* for the **analog dominant** configuration.

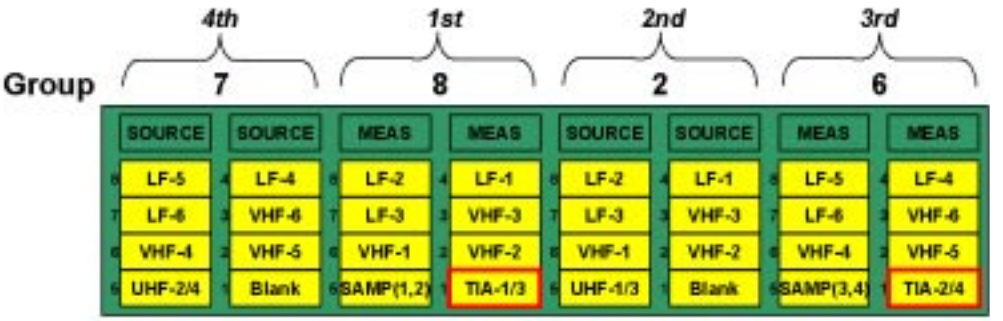


Figure 41 Fill Order of Analog Instruments within the Analog Dominant Configuration

In *Figure 41*the eight lightly shaded (yellow) boxes are the half groups of the four groups which can support analog instrument within the 1024 pin analog dominant configuration. Thus, for this configuration the analog instruments can only be placed in those card cages corresponding to groups 2, 6, 7 and 8. In the case of the 512 pin digital dominant configuration, the analog instruments can only go in the card cage slots corresponding to groups 2 and 8.
The analog time analysing or measuring instruments go in the half groups titled **MEAS**. The analog signal generators go in the half groups titled **SOURCE**. Depending on the half group, the abbreviations of analog instruments correspond to either **source** or **measurement** in the table in *Table 5*. The numbers next to an abbreviation assign the counting number of an instrument type. These count numbers increase with increasing filling of the cages. The fill order of the cages is marked above the brackets on top of the group sketches. The slot number of the slots where an analog module has to go within the cage is mentioned on the left of the half groups.

A **TIA** test head card always comes with a GP TIA and either with a second GP TIA or optionally with a HP-TIA. The first card containing a GP TIA is placed in slot 1 of group 8 as the second one goes in the first slot of group 6. In each of the two slots you can chose one of the two

optional TIAs on top (marked “slot b” in the table in *Table 7*). This way you can obtain a maximum number (MAX) of 4 GP TIAs. Otherwise, you can have up to 2 HP TIAs but in this case only 2 GP TIAs.

In the case of the sampling instruments, there are two samplers in a slot as the **sampler**s are **dual** and thus two count numbers each are assigned in *Figure 41*. Therefore the maximum number of single samplers is additionally mentioned in brackets in the table in *Table 7*.

The **Blank** slots in *Figure 41* are kept for future enhancements.

Source	1st	2nd	3rd	4th	5th	6th	Max
LF-AWG	group 2 slot 4	group 2 slot 8	group 2 slot 7	group 7 slot 4	group 7 slot 8	group 7 slot 7	6
VHF-AWG	group 2 slot 6	group 2 slot 2	group 2 slot 3	group 7 slot 6	group 7 slot 2	group 7 slot 3	6
UHF-AWG	group 2 slot 5a	group 2 slot 5b	group 7 slot 5a	group 7 slot 5b			4
Measure							
LF-DGTZ	group 8 slot 4	group 8 slot 8	group 8 slot 7	group 6 slot 4	group 6 slot 8	group 6 slot 7	6
VHF-DGTZ	group 8 slot 6	group 8 slot 2	group 8 slot 3	group 6 slot 6	group 6 slot 2	group 6 slot 3	6
SAMP (2)	group 8 slot 5	group 8 slot 5					2(4)
GP-TIA	group 8 slot 1a	group 8 slot 1a	group 8 slot 1b	group 6 slot 1b			2(4)
HP-TIA	group 8 slot 1b	group 8 slot 1b					2(0)

Table 7 Analog Instruments, Count and Filling Algorithm for the Analog Dominant Configuration

The numbers in the head row of *Table 7* assign the count numbers of the analog instruments.

DPS-Type Fill Order

As illustrated in *Figure 42* on page 86, on a **1024** pin SOC DUT board, there are **eight** blocks of DPS pogo pads and **four** DPS blocks on a **512** pin SOC DUT board. As you can see in the figure there is always one DPS pogo pad block per group (black areas).

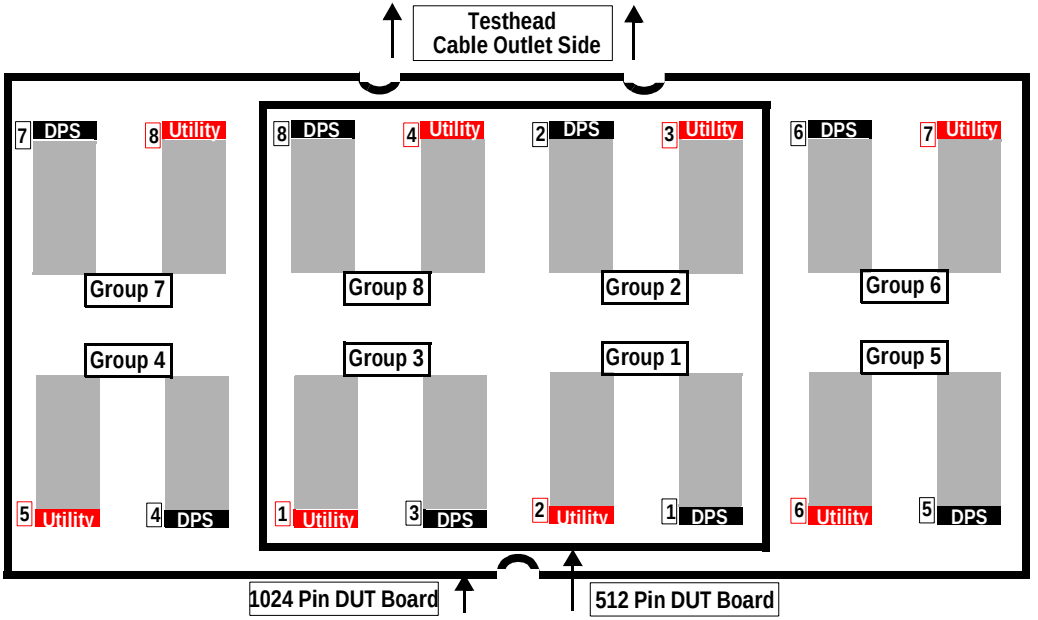


Figure 42 Position and Numbering of DPS Pogo Pad Blocks

(see also drawings **D-E6980-96540-1S34D** (512 pins) and **D-E6980-96550-1S34D** (1024 pins)

In the DPS pad blocks pogo pads of the following four different types of Device Power Supplies (DPS) can reside:

1. **GP DPS** (General Purpous DPS)
2. **LN DPS** (Low Noise DPS for analog testing)
3. **HC DPS** (High Current DPS)
4. **HV DPS** (High Voltage DPS)

A DPS block each requires a DPS card in the affiliated card cage of groupe where the DPS block resides.

DPS-Types	DPS Card Count	Filling Priority
GPDPS	1	5
	2	8
	3	9
	4	12
	5	15
	6	16
	7	17
	8	18
LN DPS	1	1
	2	2
	3	3
	4	4
HC DPS	1	6
	2	10
	3	13
HV DPS	1	7
	2	11
	3	14

Table 8 DPS-Type Filling Priority

Digital Dominant								
DPS-Type	**Group 1**	**Group 2**	**Group 3**	**Group 4**	**Group 5**	**Group 6**	**Group 7**	**Group 8**
GP DPS	1	2	3	4	5	7	6	8
LN DPS						2	3	1
HC DPS	5	4	1	3	2	7	6	8
HV DPS	5	4	1	3	2	7	6	8

Table 9 DPS-Types Sub-Sequent Filling Allgorithm, Digital Dominant Configuration

Analog Dominant								
DPS-Type	**Group 1**	**Group 2**	**Group 3**	**Group 4**	**Group 5**	**Group 6**	**Group 7**	**Group 8**
GP DPS	1	2	3	4	5	7	6	8
LN DPS						3	4	1
HC DPS	5	4	1	3	2	7	6	8
HV DPS	5	4	1	3	2	7	6	8

Table 10 DPS-Types Sub-Sequent Filling Allgorithm, Analog Dominant Configuration

Pogo Pad Assignment

This section assigns the pogo pads for the analog modules , the DPS and the utility lines in:

- *"Analog Pogo Pad Location"* on page 89.
- *"DPS Pogo Pad Functional Assignment"* on page 93.
- *"Utility, EEPROM and HPMU"* on page 97.

Analog Pogo Pad Location

The pogo pads for the AWGs the Digitizers and the TIAs are assigned in the following three parts. Here a list of some of the abreviations used in the following three tables:

- **DGND** stands for digital ground.
- **AGND** stands for analog ground.
- **FGND** stands for floating ground, i.e. no connection to any ground. These ones are kept for future expansion.
- **A+/- (B+/-,C+...)** stand for differential output lines which are used as twisted pairs each to reduce noise.
- **Sync clk** runs a trigger signal and will be used for serial inputs together with the .
- **Sync data** is thought to serve the timing generator via a two wired system with serial input after future software extensions will have been made.
- **Status out** marks whether a sampling or waveform generating process is on or off.
- **Pad #** is the number of a pad within a pad block.

(For deeper insight in the mode of operation of the analog modules see Chapter 7 *"Analog Modules"* on page 183).

1 The pogo pad assignment for the AWGs is illustrated in *Table 11*.

Pad #	GND Pad	LF-AWG	VHF-AWG	UHF-AWG
1	DGND	Status out	Status out	Ch2 marker
2	DGND			Ch1 marker
3	DGND	Sync data	Sync data	Ch2 trigger
4	DGND	Sync clk	Sync clk	Ch1 trigger
5	FGND			
6	FGND			
7	AGND			
8	AGND			
9	AGND	D- out/ D+ out	D- out/ D+ out	Ch3/4 B- out
10	AGND	D+ out	D+ out	Ch3/4 B+ out
11	AGND	C- out/ C+ out	C- out/ C+ out	Ch3/4 A- out
12	AGND	C+ out	C+ out	Ch3/4 A+ out
13	AGND	B- out/ B+ out	B- out/ B+ out	Ch1/2 B- out
14	AGND	B+ out	B+ out	Ch1/2 B+ out
15	AGND	A- out / A+ out	A- out / A+out	Ch1/2 A- out
16	AGND	A+ out	A+ out	Ch1/2 A+ out
17	AGND			

Table 11 AWG Pogo Pad Assignment

The UHF AWG's mode of operation differs from that of the other two AWG's: instead of an open collector status out signal, a single wired "marker" mentioned in *Table 11* states whether a waveform generating process is on or off.

2 The pogo pin assignment for the Digitizers is illustrated in *Table 12*.

Pad #	GND Pad	LF-DGTZ	VHF-DGTZ	SAMP
1	DGND	Status out		Status out
2	DGND			
3	DGND	Sync data		Sync data
4	DGND	Sync clk	Sync clk	Sync clk
5	FGND			
6	FGND			
7	AGND			
8	AGND			
9	AGND	D- in/ D+ in	D- in/ D+ in	
10	AGND	D+ in	D+ in	Ch2 B in
11	AGND	C- in/ C+ in	C- in/ C+ in	
12	AGND	C+ in	C+ in	Ch2 A in
13	AGND	B- in/ B+ in	B- in/ B+ in	
14	AGND	B+ in	B+ in	Ch1 B in
15	AGND	A- in / A+ in	A- in / A+ in	
16	AGND	A+ in	A+ in	Ch1 A in
17	AGND			

Table 12 Digitizer Pogo Pad Assignment

As the samplers are dual, the inputs for one sampling unit come in via channel 1 (Ch1) while the inputs for the second sampling unit come in via channel 2 (Ch2) (see *Table 12*). Both samplers within the dual sampler operate synchronously and, therefore, use the same Sync clk trigger, Sync data and Status out.

According to drawings D-E6980-96540-1S24D (512 pins) and D-E6980-96550-1S24D (1024 pins)

3 The pogo pin assignment for the TIAs is illustrated in *Table 13*.

Pad #	GND Pads	TIA
1	DGND	Trigger-2(Arm-2)
2	DGND	Trigger-1(Arm-1)
3	GND-7	Loopback-7
4	GND-7	Input-7
5	GND-6	Loopback-6
6	GND-6	Input-6
7	GND-5	Loopback-5
8	GND-5	Input-5
9	GND-4	Loopback-4
10	GND-4	Input-4
11	GND-3	Loopback-3
12	GND-3	Input-3
13	GND-2	Loopback-2
14	GND-2	Input-2
15	GND-1	Loopback-1
16	GND-1	Input-1
17	tbd	Reserved

Table 13 TIA Pogo Pad Assignment

As there are always two TIAs connected to one frontend, Trigger 1 and Trigger 2. You will need the triggers if you want to use an external arm for your time interval analysis.

The ground of each input and loop back pin within the TIAs is seperated from other inputs to reduce noise to AWG and Digitizer. Therefore, there are 7 seperate grounds.

DPS Pogo Pad Functional Assignment

Explanation of parts of drawings D-E6980-96540-1S24D (512 pins) and D-E6980-96550-1S24D (1024 pins)

The functional assignment of the DPS pogo pads for the GP DPS and the HV DPS differs from that of the LN DPS and as well from that of the HC DPS. Therefore, this section is divided into three parts according to their different functional assignments :

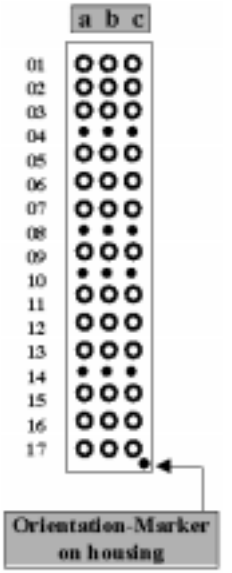
1. GP DPS and HV DPS
2. HC DPS
3. LN DPS

NOTE Since LN DPS is planned for future application, the functional assignment of these popo pads is **preliminary**.

For the amount how many DPS pogo pad blocks of each DPS-type are possible and for the filling priority of the four DPS-types see *"DPS-Type Fill Order"* on page 86. For details on the DPS-types (general description, performance and specifications) refer to Chapter 6 *"Device PowerSupply"* on page 135.

GPDPS and HVDPS, Functional Assignment of Pogo Pads

In *Table 14* the functional assignment of the DPS pogo pads either for the **GP DPS** or the **HV DPS** is illustrated. Additionally, the layout of a GP DPS or HV DPS block is illustrated on the left of the table. In *Table 14*, **a**, **b** and **c** refer to the three columns of 17 DPS pads each.



Row #	a	b	c
1	G1	G1	G1
2	GS1	GRD1	PS1
3	P1	P1	P1
4	NC	NC	NC
5	G2	G2	G2
6	GS2	GRD2	PS2
7	P2	P2	P2
8	NC	NC	NC
9	TR+	TRVB-	VB+
10	NC	NC	NC
11	G3	G3	G3
12	GS3	GRD3	PS3
13	P3	P3	P3
14	NC	NC	NC
15	G4	G4	G4
16	GS4	GRD4	PS4
17	P4	P4	P4

Table 14 Functional Assignment of the GP DPS and the HV DPS Pogo Pads and Layout of a DPS Pogo Pad Block.

Each GP DPS or HV DPS block supports four channels which consist of three power lines **P**, three ground lines **G**, a power sense line **PS**, a ground sense line **GS** and a gard line **GRD** each.

There are always three power pads ganged in one channel. The available maximum current per channel is:

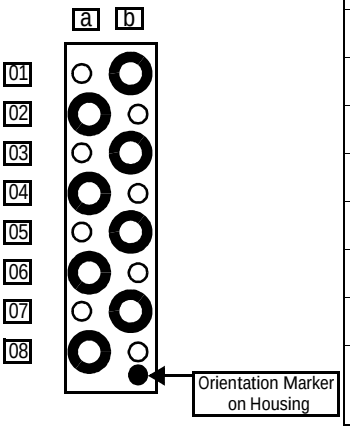
- *8 A* for the GP DPS.
- *1 A* for the HV DPS.

Not available on the wafer prober DUT board

The trigger line **TR+** is reserved for a measurement initiation in a future extension.
VB+ is a so called voltage bump. VB+ is a hardware triggered switch which allows you to change the voltage to a different value. The advantage of a hardware controlled switch rather than a software controlled switch is that the point of time of the voltage change is well defined.
TRVB- is the ground of VB+ and TR+.
The pads in rows 4, 9 and 14 (small black dots) are Not Connected (**NC**).

High Current DPS , Functional Assignment of Pogo Pads

In *Table 15*, the functional assignment of the HC DPS pogo pads is illustrated.



Pogo Pad (Pin) No.	a	b
01	Current_Monitor	G1
02	P1	V trig
03	V bump	G1
04	P1	SAFETY_LINE
05	PS1	G1
06	P1	GS1
07	SGND	G1
08	P1	+5V

Table 15 Functional Assignment of the High Current DPS Pads

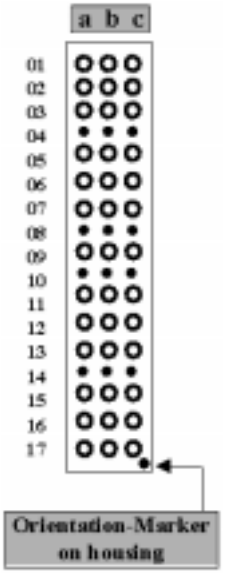
The HC DPS pogo pad blocks as sketched on the side of *Table 15* have less pogo pads. Those pads for the ground (**G**) and the power lines (**P**) are larger in diameter and

therefore there are fewer pogo pads in the High Current DPS pogo pad blocks then for the other DPS-types (LN DPS, GP DPS and HV DPS). This has to be considered designing your DUT boards.

Preliminary Pogo Pad Functional Assignment of LN DPS

In *Table 16*, the **preliminary** functional assignment of the future LN DPS is illustrated. For the abbreviations used there, see the description of the functional assignment of the GP DPS and the HV DPS at the beginning of this section. Additionally, **TR1-2** are 2 **TR**igger lines and **TR-G** stands for **TR**igger **G**round.

On the left side of the table, the layout of an LN DPS is shown. The small black dots there are pogo pads which are Not Connected (**NC**).



Row #	a	b	c
1	G1	G1	G1
2	GS1	GRD1	PS1
3	P1	P1	P1
4	NC	NC	NC
5	G2	G2	G2
6	GS2	GRD2	PS2
7	P2	P2	P2
8	NC	NC	NC
9	TR+	TRVB-	VB+
10	NC	NC	NC
11			
12			
13			
14	NC	NC	NC
15			
16			
17			

Table 16 Functional Assignment of the LP DPS Pogo Pads and Layout of a DPS Pogo Pad Block.

Utility, EEPROM and HPMU

According to drawings D-E6980-96540-1S24D (512 pins) and D-E6980-96550-1S24D (1024 pins) For utility pads on the probe card see *Table 23* and *Table 24* on page 112.

The Read/Write utility lines allow you to control external devices such as relays, solenoids or indicators, depending on the application. The utility lines are implemented as open collector output with a maximum current of 75 mA and a maximum voltage of 50 V.

NOTE Utility lines are not affected by standard connect/disconnect sequences but only controlled by dedicated test function/firmware commands. This allows the utility line to assume a steady state setup *before* the actual testflow takes control, and to remain in this state *even* after test execution has been completed.

The functions of the utility pads of the 512 pin and the 1024 pin SOC series DUT boards are illustrated in *Table 17* and *Table 19*. For the position and numbering of the utility blocks see *Figure 42* on page 86.

NOTE The numbering of the utility blocks differs from the numbering of the DPS blocks which is the same as for the groups.

In *Table 17* and *Table 19*, **a** and **b** refers to the two columns of 17 pads each of a utility block (see also the drawing of a utility block on the left of *Table 17*).

The utility pads have got the following functions:

- **URW#** are the Utility Read-Write lines.
- **UW#** are the Utility Write-Only lines.
- **UGND** is the Utility Ground which is isolated from the system GND to avoid noise.
- **UP5V** is the 5 V power supply.

- **DSC** states when the DUT board is Disconnected and when it has been taken off the test head. DSC has to be routed to UGND.

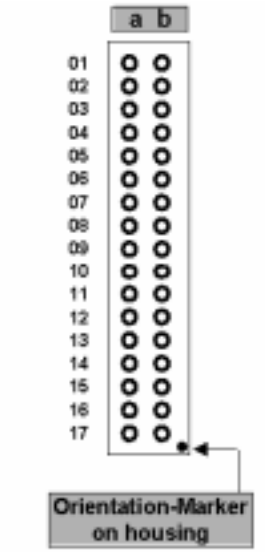
The utility block ground pins (**UGND**) are isolated from the system GND to avoid noise.

The four pad functions which are surrounded by a box in *Table 17* and *Table 19*, are connections for the High Precision Parametric Measurement Unit (**HPMU**). The functions are as follows::

- **PDCF** is for the DC Force.
- **PDCS** is the DC Sense.
- **PGDS** is the Ground Sense.
- **PGRD** is the Gard line.

In *Table 18* and *Table 20* you can find the assignment of which HPMU connects to which utility block.

NOTE These HPMU connections are optional. Even without connecting the force line directly via a fixed wire with a signal line on the DUT you can perform HPMU measurements on any signal pin. This works by switching relays to connect any signal line on the DUT with the HPMU. But this way you don't have any gard or sense lines.



Pin No.	Utility block 1		Utility block 2, 3, 4	
	a	b	a	b
1	URW00	UGND	UW00	UGND
2	UGND	URW01	UGND	UW01
3	URW02	URW03	UW02	UW03
4	URW04	UP5V	UW04	UP5V
5	UP5V	URW05	UP5V	UW05
6	URW06	UW07	UW06	UW07
7	UW08	UGND	UW08	UGND
8	DSC	UW09	DSC	UW09
9	UW10	UGND	UW10	UGND
10	UGND	UW11	UGND	UW11
11	UW12	UGND	UW12	UGND
12	UGND	UW13	UGND	UW13
13	URW14	UGND	UW14	UGND
14	UGND	URW15	UGND	UW15
15	PDCS	PDCF	PDCS	PDCF
16	PGDS	PGRD	PGDS	PGRD
17	NC	NC	NC	NC

Table 17 Function of Utility Pogo Pads (512 pin DUT board)

Utility Block No.	1	2	3	4
HPMU No.	12	21	22	11

Table 18 Assignment: Connections of which HPMU (SPMU)are located on which Utility Block

Pin No.	Utility block 1		Utility blocks 3, 5, 7		Utility blocks 2, 4, 6, 8	
	a	b	a	b	a	b
1	URW00	UGND	UW00	UGND	URW00	UGND
2	UGND	URW01	UGND	UW01	Reserved	URW01
3	URW02	URW03	UW02	UW03	URW02	URW03
4	URW04	UP5V	UW04	UP5V	URW04	UP5V
5	UP5V	URW05	UP5V	UW05	UP5V	URW05
6	URW06	UW07	UW06	UW07	URW06	UW07
7	UW08	UGND	UW08	UGND	UW08	UGND
8	DSC	UW09	DSC	UW09	DSC	UW09
9	UW10	UGND	UW10	UGND	UW10	Reserved
10	UGND	UW11	UGND	UW11	UGND	UW11
11	UW12	UGND	UW12	UGND	UW12	Reserved
12	UGND	UW13	UGND	UW13	Reserved	UW13
13	URW14	UGND	UW14	UGND	URW14	Reserved
14	UGND	URW15	UGND	UW15	UGND	URW15
15	PDCS	PDCF	PDCS	PDCF	PDCS	PDCF
16	PGDS	PGRD	PGDS	PGRD	PGDS	PGRD
17	NC	NC	NC	NC	NC	NC

Table 19 Function of Utility Pogo Pads (1024 pin DUT board)

Utility Block No.	HPMU No.	Utility Block No.	HPMU No.
1	12	5	42
2	21	6	31
3	22	7	32
4	11	8	41

Table 20 Assignment : Connections of which HPMU are located on which Utility Block

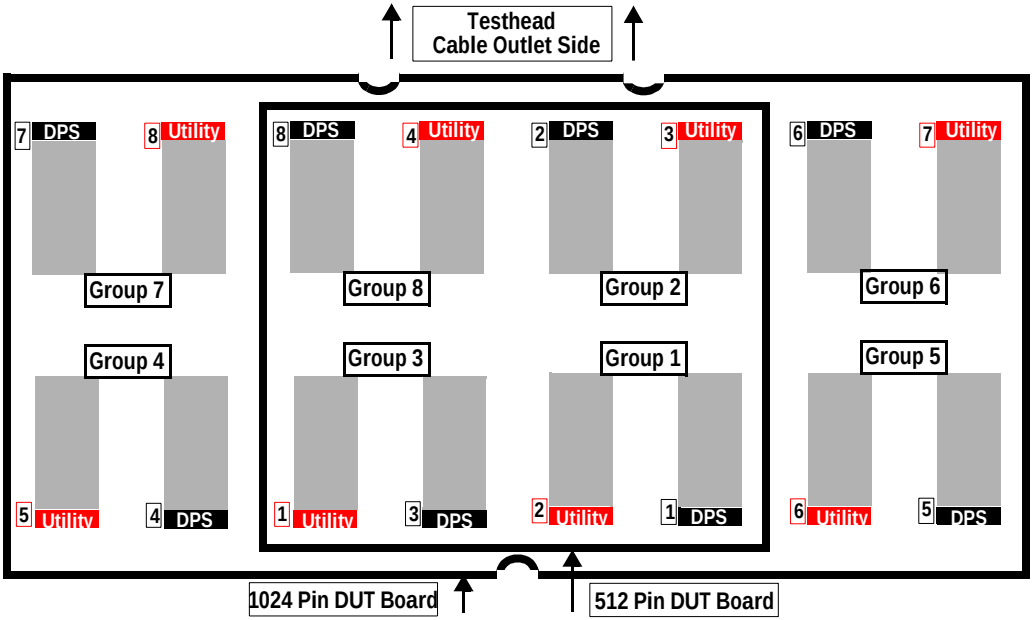


Figure 43 Position and Numbering of Utility Blocks
(see also drawings **D-E6980-96540-1S34D** (512 pins) and **D-E6980-96550-1S34D** (1024 pins)

EEPROM

Via the utility lines of utility block 1 you can read the XICOR (manufacturer) EEPROM, partnumber X24C04, package 8-pin SOIC. You can use this EEPROM to identify the DUT board. *Figure 44* shows the possible positions of the EEPROM on both, the 512 pin and the 1024 pin DUT Board. Normally, for wiring reasons, the EEPROM would be placed on the right side of utility block 1 (see the figure).

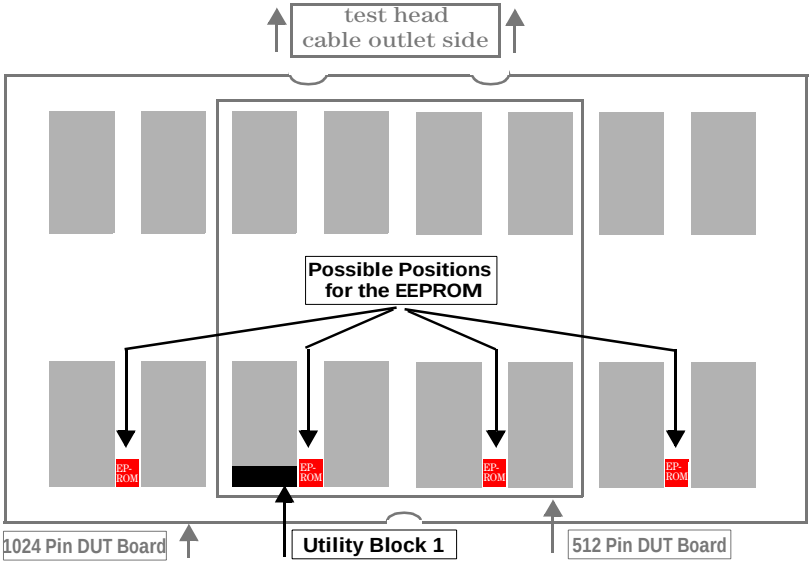


Figure 44 Possible Positions for EEPROM on DUT Board - View from DUT Side

Table 21 shows, which of the EEPROM pins connect to which pogo pad of utility block 1. The there used abbreviations for the functional assignment of the pins have the following meaning:

- **SCL** is the pin for the **S**erial **CL**ock.
- **SDA** is the pin for **S**erial **DA**ta.
- **A1** and **A2** are the **A**ddress inputs pins, **A0** is a no connect pin.
- **VSS** is the ground pin
- **WPI** is the test input pin.
- **VCC** is the supply voltage pin.

For a summary of the EEPROM by the producer (XICOR) see the Appendix A *"XICOR EEPROM Summary"* (p. 267).

Utility Block 1		EEPROM X24C04	
Utility Pad Name	**Utility Pad Functional Assignment**	**EEPROM Pin Functional Assignment**	**EEPROM Pin Numbering**
13a	URW14	SCL	6
14b	URW15	SDA	5
14a	UGND	A0	1
14a	UGND	A1	2
14a	UGND	A2	3
14a	UGND	VSS	4
14a	UGND	WPI	7
05a	UP5V	VCC	8

Table 21 Functional Assignment of EEPROM Pins and Assignment of EEPROM Pins to Utility Pads of Utility Block 1

Wafer Prober DUT Board and Probe Card

In *Figure 45* on page 104, the position of the wafer prober DUT board and the probe card above the test head is illustrated. You will find an overview of the wafer prober DUT board in *"DUT Board of Wafer Prober"* on page 105 . In section *"Probe Card-Pogo Pad Assignment"* on page 107 you are given an overview of the pogo pad assignment from probe card view.

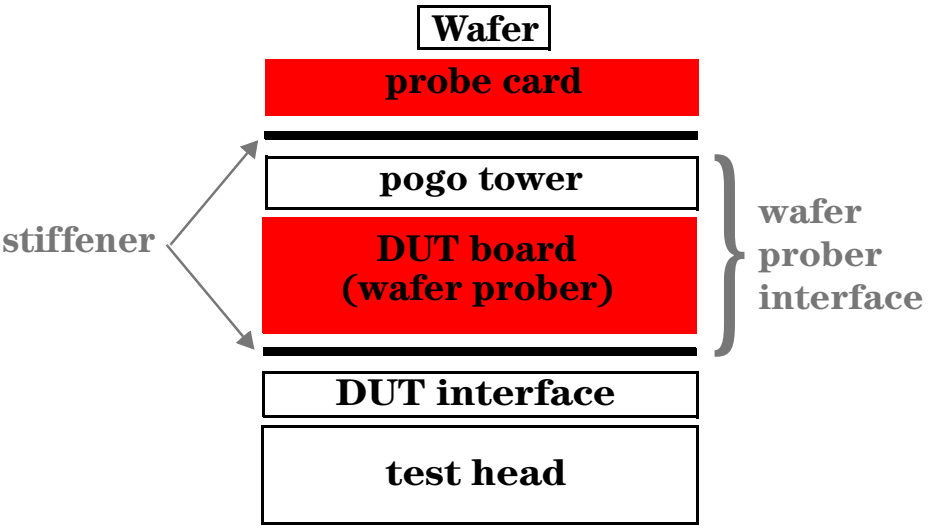


Figure 45 Position of Wafer Prober DUT Board and Probe Card above the Test Head

DUT Board of Wafer Prober

See also drawings D-E7018-96504-1S12B (512 pins) and D-E7018-96501-1S12B (1024 pins)

For the SOC pogo tower there are two wafer prober DUT boards:

1. a **512** pin wafer prober DUT board.
2. a **1024** pin wafer prober DUT board.

In *Figure 45* on page 104, you are given a schematic drawing of an 1024 pin wafer prober DUT board. The area surrounded with the black line in the middle of the 1024 pin wafer prober DUT board is equivalent to a 512 pin wafer prober DUT board.

The heavily shaded grey boxes in the two rows, one in the top and the other in the bottom half of the illustrated board, are so called **half group**s. These half groups are the areas where the pogo pads connect to the test head via the DUT interface. A half group each consists of four pairs of **pad block**s of 17 signal lines each, see also *"Pad Blocks"* on page 67. Additional, each half group contains pads for the DPS and for the utility lines.

Always two of these rectangularly arranged half groups of pogo pads are projected to one **segment** in the circularly shaped area in the middle of the wafer prober DUT board. Each segment only contains pogo pads of those two half groups which build a group. For the numbering of the groups see *Figure 32* on page 65 which is the same as of the probe card segments (see *Figure 47* on page 107).

In case of the 512 pin DUT board only the four black segments are in use as this wafer prober DUT board only consists of the four groups of pogo pads of the area surrounded in black.

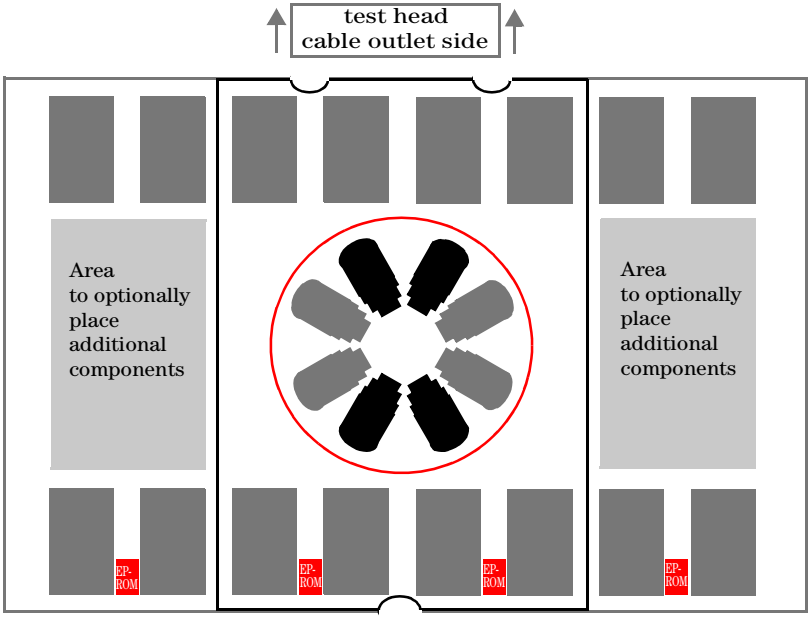


Figure 46 Schematic Drawing of Wafer Prober DUT Board Layout - View from DUT Side

As the circular area is limited in space and for ground reasons, as far as the signal lines are concerned, you have to decide either for digital only or analog only signal lines within a single group/segment each. Note, that you can only have analog signal lines in some of the groups depending on your test system configuration and your test head filling (see *"Test System Configuration"* on page 70). For the pogo pad assignment of the segments see the description of the prob card in *"Probe Card-Pogo Pad Assignment"* on page 107.

To know, which group connects to which card cage in the test head see *"DUT Board Mechanical Considerations"* on page 61.

Probe Card-Pogo Pad Assignment

See the same drawing as in *"DUT Board of Wafer Prober"* on page 105

In *Figure 47* on page 107, you are given a schematic drawing of a probe card.

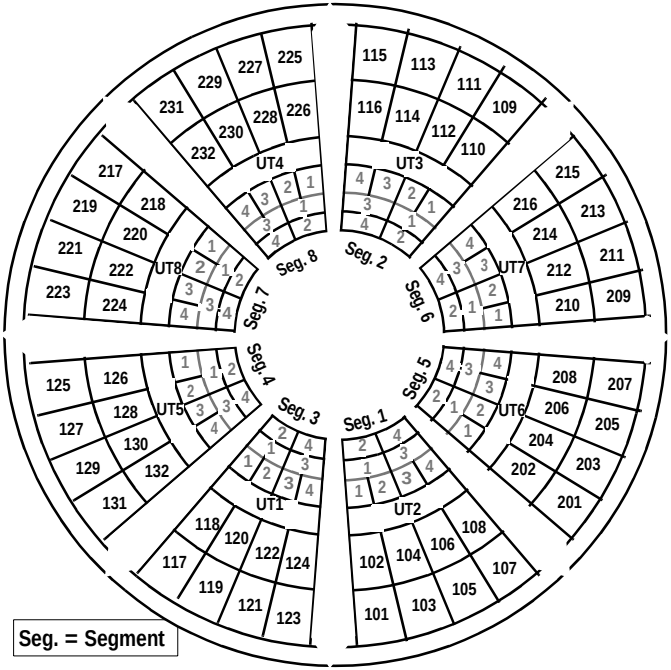


Figure 47 Schematic Drawing of Probe Card- View from DUT Side

In *Figure 47* on page 107now, you can see the general structure of the eight probe card segments. Each segment consists of smaller units indicated by the lines.

signal line pogo pads

The units with the **black numbers** away from the circle's center contain the pogo pads for the signal lines.

utility line pogo pads

The units named **UT1-8** are the areas where the pogo pads of the utility lines are placed.

DPS pogo pads

The units next to the center of the probe card with the **grey numbers** are for the DPS pogo pads: Those four units next to the utility lines contain the ground and the power lines of the four DPS channels 1-4, while the four units next to the center of the probe card contain the gard lines, power and ground sense lines and the ground lines of channels 1-4.

For a detailed description of a probe card segment see *"General Structure of a Probe Card Segment"* on page 108.

General Structure of a Probe Card Segment

See also the drawing D-E7018-96502-1S11B

In *Figure 48* on page 108, the general structure of all probe card segments is illustrated.

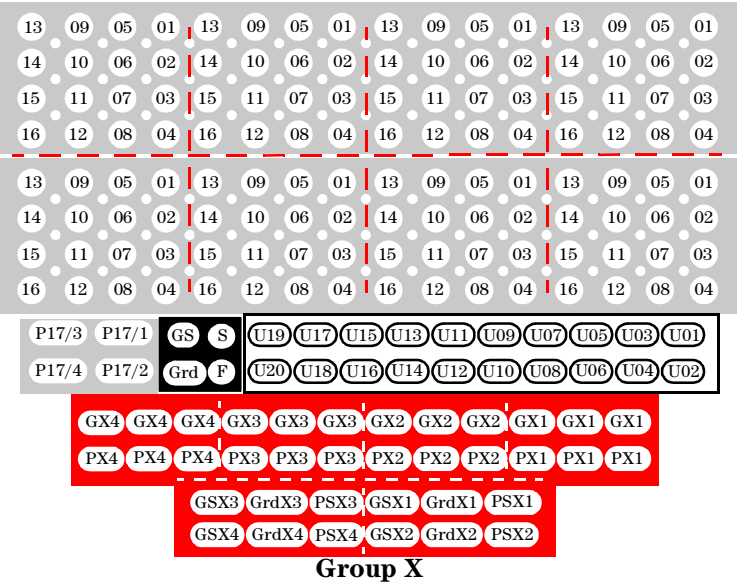


Figure 48 General Structure of a Probe Card Segment

input-output pogo pads on the probe card

The **lightly shaded grey area** of *Figure 48* on page 108 contains the pogo pads of the input -output signal lines (circles with numbers).

The small white dots between the signal pads are the ground pads.

The area consists of 8 **unit**s as indicated by the dashed lines.

Each unit contains 16 of those signal lines.

The pogo pads of the signal lines contained in one unit are all connected to the same pogo pad block within the groups on the wafer prober DUT board.

The numbers given to each unit are shown in *Figure 47* on page 107. These numbers are the same as for their origin pogo pad blocks within the groups on the wafer prober DUT board. For the numbering of the pogo pad blocks within the rectangularly shaped groups see *Figure 31* on page 64(512 pins) and *Figure 32* on page 65(1024 pins). Though, the numbering of the pogo pad blocks is illustrated for packaged parts DUT boards, there, it is the same for the wafer prober DUT boards.

The signal line pogo pads of the units are given the same numbers (see *Figure 48* on page 108) as for the pogo pads of the signal line pogo pads within the the pad blocks (see *Figure 33* on page 67).

17th signal lines on the probe card

In *Figure 33* on page 67, additionally, a 17th signal line is illustrated. Four of the eight 17th signal lines of a group each are also available on a probe card segment. They are placed in the smaller lightly shaded grey area on the left side of the white area. *Table 22* shows the numbers of the pairs of pogo pad blocks the four 17th signal lines connect to within the groups.

Naming of 17th Signal Lines on Probe Card	No. of Pogo Pad Block							
P17/1	105	113	121	129	205	213	221	229
P17/2	106	114	122	130	206	214	222	230
P17/3	107	115	123	131	207	215	223	231
P17/4	108	116	124	132	208	216	224	232
Segment (Group) No. :	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**

Table 22 Pogo Pad Block Assignment of the 17th Signal Lines of the Segments on the Groups of the Packaged Parts DUT Board

If the signal lines connect to the block of the analog pogo pads or to the digital pogo pad block of one pair of pogo pad blocks (see *"Pad Blocks"* on page 67), depends on your customized wafer prober DUT board and heavily on your test head configuration (see *"Test System Configuration"* on page 70).

NOTE Within one segment you can only have digital or analog signal lines since there is only one ground (either digital or analog). (If you are using the standard SOC wafer prober DUT board, (E7018AA or E7018AB), all signal lines connect to the digital pogo pad blocks.

utility line pogo pads on the probe card

The **white area** of *Figure 48* on page 108 contains the pogo pads of the **utility lines**. The functions of the pogo pads numbered from U01 to U20 are listed in *Table 23* for the 512 pin probe card and in *Table 24* for the 1024 pin probe card.

Naming of Utility Pogo Pads on Probe Card	Function of the Utility Pogo Pads			
U01	UG	UG	UG	UG
U02	URW00	UW00	UW00	UW00
U03	URW01	UW01	UW01	UW01
U04	URW02	UW02	UW02	UW02
U05	URW03	UW03	UW03	UW03
U06	URW04	UW04	UW04	UW04
U07	5V	5V	5V	5V
U08	5V	5V	5V	5V
U09	URW05	UW05	UW05	UW05
U10	URW06	UW06	UW06	UW06
U11	UW07	UW07	UW07	UW07
U12	UW08	UW08	UW08	UW08
U13	UG	UG	UG	UG
U14	UW09	UW09	UW09	UW09
U15	UW10	UW10	UW10	UW10
U16	UW11	UW11	UW11	UW11
U17	UW12	UW12	UW12	UW12
U18	UW13	UW13	UW13	UW13
U19	URW14	UW14	UW14	UW14
U20	URW15	UW15	UW15	UW15
Utility Block Number	**UT1**	**UT2**	**UT3**	**UT4**
Segment (Group)	**3**	**1**	**2**	**8**

Table 23 Functional Assignment of the Utility Pogo Pads of 512 Pin Probe Card

Naming of Utility Pogo Pads on Probe Card	Function of the Utility Pogo Pads							
U01	UG	UG	UG	UG	UG	UG	UG	UG
U02	URW00	URW00	UW00	URW00	UW00	URW00	UW00	URW00
U03	URW01	URW01	UW01	URW01	UW01	URW01	UW01	URW01
U04	URW02	URW02	UW02	URW02	UW02	URW02	UW02	URW02
U05	URW03	URW03	UW03	URW03	UW03	URW03	UW03	URW03
U06	URW04	URW04	UW04	URW04	UW04	URW04	UW04	URW04
U07	5V	5V	5V	5V	5V	5V	5V	5V
U08	5V	5V	5V	5V	5V	5V	5V	5V
U09	URW05	URW05	UW05	URW05	UW05	URW05	UW05	URW05
U10	URW06	URW06	UW06	URW06	UW06	URW06	UW06	URW06
U11	UW07	UW07	UW07	UW07	UW07	UW07	UW07	UW07
U12	UW08	UW08	UW08	UW08	UW08	UW08	UW08	UW08
U13	UG	UG	UG	UG	UG	UG	UG	UG
U14	UW09	UW09	UW09	UW09	UW09	UW09	UW09	UW09
U15	UW10	UW10	UW10	UW10	UW10	UW10	UW10	UW10
U16	UW11	UW11	UW11	UW11	UW11	UW11	UW11	UW11
U17	UW12	UW12	UW12	UW12	UW12	UW12	UW12	UW12
U18	UW13	UW13	UW13	UW13	UW13	UW13	UW13	UW13
U19	URW14	URW14	UW14	URW14	UW14	URW14	UW14	URW14
U20	URW15	URW15	UW15	URW15	UW15	URW15	UW15	URW15
Utility Block Number	**UT1**	**UT2**	**UT3**	**UT4**	**UT5**	**UT6**	**UT7**	**UT8**
Segment (Group) No.	**3**	**1**	**2**	**8**	**4**	**5**	**6**	**7**

Table 24 Functional Assignment of the Utility Pogo Pads of 1024 Pin Probe Card

The abbreviations of the utility pogo pad functions of *Table 23* and *Table 24* hve the following meaning:

- **##** is the numbering of the read and write or write only utility lines. Thus there are 15 utility lines per segment. This numbering is consistent with the numbering of the utility lines on the packaged parts DUT boards which is illustrated in *Table 17* on page 99 and *Table 19* on page 100.
- **URW** stands for **R**ead and **W**rite ability of the 15 utility lines of the assigned segments.
- **UW** stands for **W**rite only ability of the 15 utility lines of the assigned segment.
- **UG** is the **U**tility **G**round.
- **5V** equals 5 Volt power supply.

As mentioned above, the numbering of the segments on the probe card and their destination groups on the rectangularly shaped DUT boards is the same, therefore the expresssion Segment (Group) No. in *Table 23* and *Table 24*.

HPMU pogo pads on the probe card

Additionally, each segment contains four pogo pads for the **H**igh precision **P**arametric **M**easurement **U**nit (**HPMU**) (**black area** in *Figure 48* on page 108). The four pogo pads there have the following function:

- **S** is the **S**ense line.
- **F** is the **F**orce line.
- **GS** is the **G**round **S**ense line.
- **Grd** is the **Gard** line.

Table 25 assigns the number of the HPMU the four lines of a segment are connected to.

Segment (Group) No. containing the PogPads of Sense, Ground Sense, Force and Gard Line	1	2	3	4	5	6	7	8
No. of HPMU	12	21	22	11	42	31	32	41

Table 25 Assignment of Sense, Ground Sense, Force and Gard Line of which Segment connect to which HPMU

The **heavily shaded grey area** in *Figure 48* on page 108 is the pogo pad area of the DPS channels.

DPS pogo pads on the probe card

The DPS pogo pad area of each segment supports four channels. Each channel consists of three **P**ower lines (**P**) which are ganged. Additionally, per channel, there are three **G**round lines (**G**).

In the lowest part of the segment,

- a **P**ower **S**ense line (**PS**),
- a **G**round **S**ense line (**GS**) and
- a **G**a**RD** line (**GRD**)

for all four DPS channels is placed.

For details on the DPS refer to Chapter 6 *"Device Power-Supply"* on page 135.

5

DUT Board Performance Considerations

This chapter provides you with information on:

Signal Traces

Landing holes/vias are **inside** the landing pads. The via-in-pad method provides better contact reliability than pogo-on-surface methods.

High-Frequency Testing

Testing at high frequencies requires an impedance-matched environment. The board should therefore be designed to match the tester impedance. For proper operation, the impedance specification of 50 Ω ±10% must be met. We recommend that you use the inner part of the board for the high-speed traces. In this area, the process tolerances are usually tighter, resulting in a better impedance matching.

A minimum trace width of 12 mil (0.3 mm) is recommended. The wider the trace width, the lower the attenuation and skin effects.

Line Insulation

All signal and ground lines and pads on the board must be insulated from the stiffener. If signal lines or pads are placed on the board's surface that touches the stiffener, an insulation sheet must be inserted between stiffener and board (max. thickness 0.2 mm). Do not exceed this thickness, as the sheet reduces the pogo travel. Recommended material is Epoxy F40 or similar. Before selecting the material, check whether the stiffener will be used at extreme hot or cold temperatures.Without insulation, these signal lines may either short on or inductively couple to the stiffener. Milling of these areas on the stiffener is not advised since this weakens the mechanical stability of the assembly.

Dummy Pads

For compatibility with future upgrades, the associated pogo area should be free of any contacts or parts on the bottom of the DUT board. We recommend that you add dummy pads so that the DUT board is usable on systems

with higher pin count. Without these dummy pads, the pogo pins of the DUT interface may damage the unprotected DUT board over time.

Typical pad size is 1.6 to 1.8 mm, hole diameter is 0.7 mm.

Landing Holes We recommend to use pogo landing holes (plated through holes) instead of plane pads for better contact quality. A landing hole provides a 3-point signal contact, whereas a plane pad has a single contact point only. Over time, abrasion will reduce the contact quality, with a plane pad this is much more critical than with a landing hole. Don't use blind vias either, as their contact quality is inferior to pogo landing holes.

Unused tester channels may have pads without holes.

DPS Lines For information of DPS line layout, refer to *"Routing DPS Lines"* on page 163.

Keep-out Areas

Care must be taken when putting traces on the board's outer side. In handler applications, the board is close to the metal of the handler and could inductively couple if not short out. Only low-speed traces should be placed on the board's outer sides, even with the additional isolation sheet.

- No traces or components are allowed on the bottom/tester side of the board (except within an area of 120×120 mm).
- Traces are allowed on the top/DUT side of the board (except landing pad and mechanical hole areas).
- The stiffener will lie flush against the bottom surface of the PCB at every point except the landing pad areas.

Maintaining Signal Fidelity

Because the tester does not limit your choice of pin-to-channel allocation, you can design the DUT board layout so that you get the best possible signal fidelity at high frequencies.

When you design a new DUT board for high-frequency test applications (or have one designed for you), you have to ensure that the board will transport the test signals to the DUT and back without appreciable loss of signal quality.

50 Ohm Impedance

Always specify and use a 50 Ohm impedance environment.

Crosstalk

Keep crosstalk down to a minimum by:

- avoiding routing long signal lines in parallel
- using maximum allowable spacing between signal lines
- minimizing the spacing between signal line and ground
- running a ground strip between two signal strip lines
- distributing signal lines through multiple board layers
- terminating strip lines with the characteristic impedance

Signal Inhomogeneities

Inhomogeneities cause reflections in the signal paths as well as signal deterioration due to attenuation and phase changes.

Minimize signal inhomogeneities by:

- avoiding runs of wire on the DUT board
- avoiding vias on the board if possible. If the use of a via is unavoidable, make sure to specify a 50 Ohm equivalent via to the custom DUT board manufacturer.
- avoiding stubs. If you must have a stub, for instance to connect a socket to a signal track, place the junction to the stub between the pogo pin and the DUT pin, and insert a surface-mounted series resistor between the junction and your socket.
- avoiding unnecessary sharp corners in strip lines. Use a radius, or a chamfered corner instead.
  avoiding mouse bites and size changes in strip lines.
- using the correct procedures when soldering coax cables to strip lines—minimize the length of unshielded core, provide a good ground connection for the coax shield.

Correctly Terminating Signal Lines

The guidelines below give you a simplified view for handling transmission lines.

Why use Impedance Matching Techniques?

At the high edge-transition speeds of the tester, traces and coaxial cables start to behave like transmission lines. If not properly terminated, every pulse transition that you send is reflected back down the line. This can cause severe distortion in the signal you are transmitting.

The way to prevent the reflections is to terminate at least one end of the line with a load which matches the characteristic impedance of the transmission line.

How Transmission Lines are Terminated

To prevent reflections in the connection between the IO Channel and the DUT, the tester uses an impedance-matched environment. This means that the coaxial cables have a characteristic impedance of 50 Ω. At the tester end, the driver in each IO channel also has an impedance of 50 Ω, used to terminate the transmission line.

Thus, all the signal-input lines to the DUT are terminated already so that if the signal frequency causes transmission line effects, they are impedance-matched to prevent any reflections. Traces on the DUT board also have to be impedance-matched.

Terminating Output Pins

Output pins are not automatically provided with termination. If you believe that the outputs from a DUT are operating fast enough to cause transmission line effects, you can add a 50 Ω termination load.

When you select termination for your DUT output, the load is provided by the driver-half of the IO channel.

Setting Termination Voltage

In general, if you use ECL-type levels, (usually –1.7 V low and –0.8 V high), set the driver (V_{term}) to –2 V in the Level setup.

Special Considerations for CMOS Outputs

Some devices (notably high speed CMOS) cannot drive into the 50 Ω provided by the coaxial cable with 50 Ω termination at the pin electronics. The solution is to use a resistive divider:

Connect a load resistor R_s directly in series with the DUT output. The output voltage of the DUT is then scaled down by a factor of:

$$\frac{50\Omega}{R_S + 50\Omega}$$

Terminating Bidirectional Pins

If you are also testing bidirectional pins at high speeds, the considerations are very similar to those for an output pin. During output cycles (DUT pin sends), termination is provided by the driver impedance and level of the IO channel connected to that pin—for as long as it is not switched to tristate. If the DUT expects other levels than the driver levels, the termination is obtained by using the active load and switching the driver to Hi Z.

Termination Checklist

50 Ohm Environment

If you are operating in a standard 50 Ω environment, no extra action is needed as far as component layout on the DUT board is concerned. You define the termination in the Level setup.

Active Load

If you terminate the line with the help of the active load, no additional action is needed as far as component layout on the DUT board is concerned. You define the active load in the Level setup.

Voltage Clamp

If you use the clamp load (useful for high-speed CMOS devices, where 50 Ohm loading cannot be used), there is no additional action needed as far as component layout on the DUT Board is concerned. You setup the voltage clamp in the Level setup.

The concept and the use of the active load and the voltage clamp are discussed in the *Standard Test Function Reference* (Part No. E7050-91013).

Series Resistor

If you use the resistive divider as a termination method, you will need space on your DUT board for the series resistor. For best results, use surface-mounted resistors due to their low lead inductance.

For information on specifying the series resistor, refer to the *Command Reference* manual (Part No. E7050-91013).

Reducing I/O Round-Trip Times

For bidirectional pins, such as data bus pins, you have to consider the total I/O round-trip time of the signal from the I/O Board to the DUT pin and back. This is because at high vector rates the signal direction changes so often so that the signals being sent from the tester may collide with data being sent by the DUT.

As a rule of thumb, you only need to consider the round-trip time as a potential problem if the switching period of the I/O pin is less than double the propagation delay of the signal path (between the tester I/O channel and the DUT pin).

If you require very fast vector rates in I/O mode, possible techniques to employ are the use of dual transmission lines, or the introduction of extra dummy cycles in your test. You will need to modify your vector files when using these techniques.

Measures

Position/rotate the DUT in the Device Area so as to shorten the tracks to bidirectional pins (if need be at the expense of tracks to one-directional pins). This means the device side where I/O pins are located should be close to DUT board pogo pin pads. The extra length of tracks needed for I or O pins will be compensated for by adjusting pin attribute delay settings or by fixture calibration.

Specify the use of high-speed DUT board material to the custom DUT board manufacturer. For instance, teflon is faster than epoxy.

DUT Board Design for Mixed-Signal Tests

The previous sections describes the information for the DUT board design focused on digital testing. This section provides information focused on mixed-signal testing.

Analog signals can be easily disrupted by pulses (for example clocks and digital signals). To avoid this problem, both signal types must be physically separated.

Therefore, designing a DUT board for a mixed-signal device requires more effort than designing a DUT board for a purely digital device.

If you develop a DUT board, you should pay attention to not only the signals but also the signal return paths (digital ground and analog ground).

Guidelines

General Guidelines

The following issues should always be considered:

- If you are using an IC socket, place it at the center of the DUT board. This helps to create signal lines of equal length which in turn support identical travelling times of generated signals, sync pulses, and response signals.
- Put a mark at pin 1 of the socket to ensure that the device is always inserted correctly.
- Take care that input and output signal lines are physically separated (they must not be conducted in parallel).
- Ensure that relays and active components can be easily replaced. This means: Use sockets and mark the correct insertion position.

- Problems will occur: Ensure that the DUT board can be easily changed and debugged.
- Ensure that the required auxiliary components do not interfere with the IC handler or waver prober. If possible, consider mounting the components on the rear of the DUT board.

Additional Mixed-Signal Guidelines

The following issues are essential for mixed-signal devices:

- Use two separate and fairly large ground planes for connecting the digital and analog ground of the device. On the DUT board, connect the two ground planes via an inductor. An inductor protects the analog ground from spikes on the digital ground.
- Ensure that all connections between digital and analog signals to their respective grounds are as short as possible.
- Separate analog and digital signals physically.
- Use impedance-matching coaxial cables at least for all high frequency or low amplitude signals. Coaxial cables will shield the signals from radiating or picking up noise. Matching the source impedance will provide maximum signal power and least distortion.
- Use separate power supply channels for supplying the digital and analog circuits of the DUT, if possible.
- Remove spikes that can be induced via the power supply. Insert bypass capacitors between the power supply pins of the DUT and ground. These capacitors should be as close to the DUT as possible.

Grounding and Signal Shielding

Grounding

Proper grounding is essential for precise measurements. Mixed-signal devices differentiate between digital and analog ground and often also between digital and analog supply voltage.

You will need two ground planes on the DUT board which are connected somewhere via an inductor as shown in the following figure:

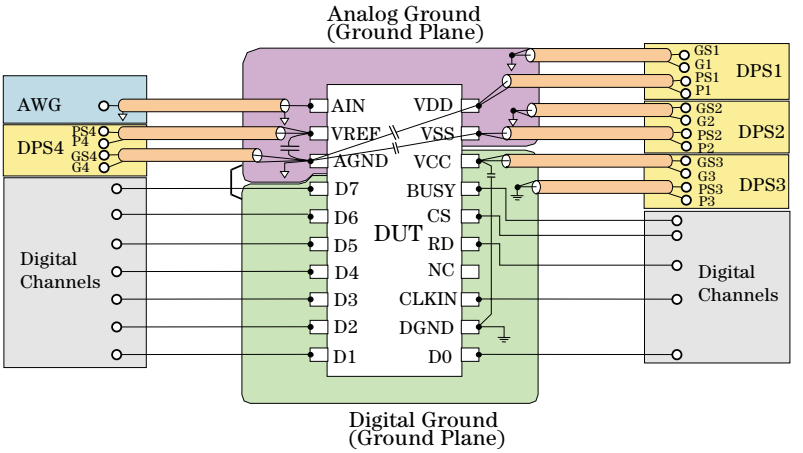


Figure 49 Digital Ground and Analog Ground

Shielding the Signals

The safest way to transport signals between analog modules and the DUT is via coaxial cables. The typical impedance is 50 Ω (except for video signals, which usually use 75 Ω).

The shields of digital signal cables must be connected to digital ground, and the shields of analog signal cables to analog ground.

Matching the impedance of the signal source should be a matter of course. This avoids reflections and is essential for all high frequency analog signals. Low voltage ECL signals, too, should only be transported by impedance matching coaxial cables.

The cable shield is normally connected to the respective analog or digital ground, except for DC signals to to from the PMU. For the PMU force and sense lines, the cable shield should be connected to guard connectors.

Notice that if you connect a coaxial cable to a high impedance input, the cable has a capacitance (depending on its dimensions, typically 100 pF/m). In high frequency applications, you may need to ensure that the signal source can drive that capacitive load.

If the requirements are not that stringent, you may also consider using twisted-pair cables or a printed circuit stripline approach (implemented by a broad ground conductor running physically just underneath the signal line).

It is always a good idea to mount and mark some test pins on the DUT board where the probe of an external instrument or oscilloscope can be attached. This will ease troubleshooting.

Filtering Supply and DC Voltage

Real world power supplies usually have a rather high impedance for high frequency load changes. That means a sudden current change of the DUT will cause a voltage spike (or drop) at the DUT supply pin.

Also, changes of the supply voltage will influence the generated or received signal and thus increase the noise level.

Use lowpass filters or at least bypass capacitors to reduce noise.

- A lowpass filter can be directly inserted into the supply lines.

- Bypass capacitors should include electrolytic and ceramic capacitors.

Electrolytic capacitors (10 µF...100 µF) cover the low frequency range.They can be positioned anywhere on the DUT board.

Ceramic capacitors (10 nF...100 nF) cover the high frequency range. They should be placed as close to the DUT pins as possible.

At the very least, the following supplies should be filtered:

- Power supply for test circuit components
- Power supply for pull-up
- Power supply for relays
- DUT reference voltage
- Termination bias voltages

Some examples for bypass capacitor connections are shown in the figure below:

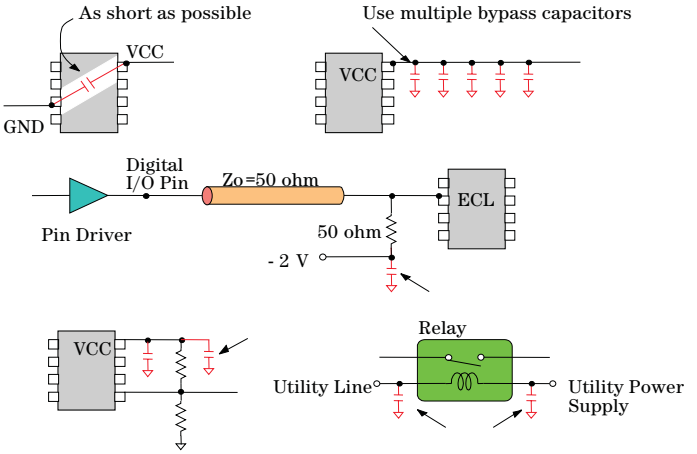


Figure 50 Bypass Capacitors

Printed Circuit Board

To run the same application on multiple testers for production tests, the DUT board is developed as a printed circuit board (PCB).

As the operation rate of a mixed-signal device increases, application engineers who develop test circuits need to be skilled not only in schematic design but also in printed circuit board design. This is because traces on the PCB at high frequency generate physical effects (reflection, crosstalk, and so on) that are not represented in the schematic.

Characteristic Impedance

According to the transmission line theory, if the characteristic impedance of a trace does not match the termination impedance and if a high-frequency signal is transmitted in the line, a reflection will occur for the signal. To measure a high-frequency signal accurately or to force a high-frequency signal accurately, the transmission line must be designed to match the termination impedance.

Hence, a microstrip line and strip line are used because their impedance can be controlled by changing the thickness, width, and height above the ground plane.

The following figure shows the model of a microstrip line:

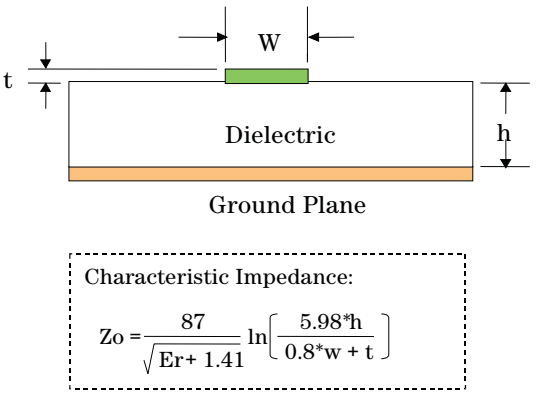


Figure 51 Microstrip Line Model

where Er means the relative dielectric constant of the board material.

The following figure shows the model of a strip line:

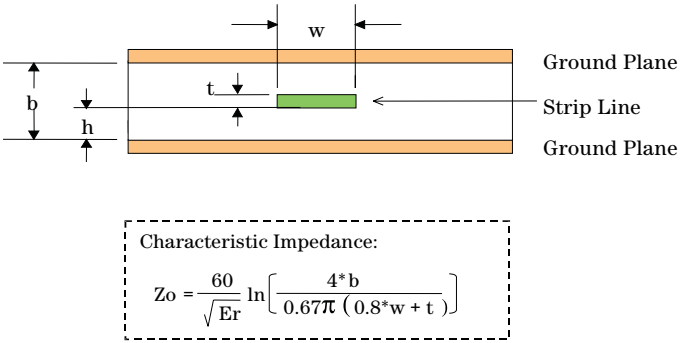


Figure 52 Strip Line Model

NOTE As shown in the above figures, the microstrip line and strip line consist of a set of a trace and ground or power plane(s). Thus, the ground or power plane(s) must not have any discontinuity under the trace.

If the number of PCB layers and the board material are determined, that is, Er, h, b, and t are determined, the only trace width, w, determines the characteristic impedance (Zo) of the transmission line.

Therefore, to design a trace correctly to be a specified impedance, pay attention to the width of the trace on the PCB. However, even if the width of a trace is exactly designed to match the termination resistor value, the following factors cause impedance mismatching:

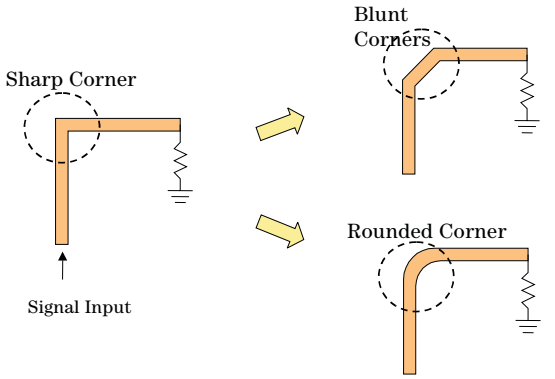


Figure 53 Sharp Corner

In the above example, if the signal frequency is very high, the sharp corner causes signal reflections. Use a blunt corner or rounded corner instead of the sharp corner.

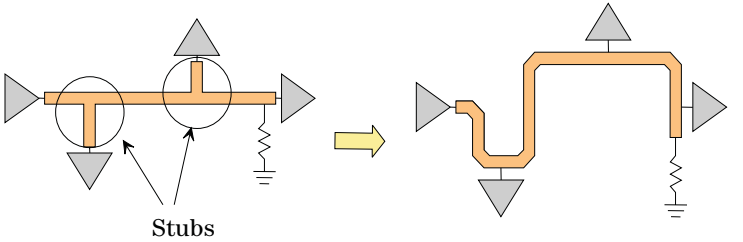


Figure 54 Branch (Stub)

In the above example, if the signal frequency is very high, these stubs cause signal reflections at the points. Consequently, the trace should be drawn without a stub.

Crosstalk

If two signal lines are traced in parallel on a PC board and if one carries a small and precise signal and the other carries a high level signal, the large signal may couple to the sensitive line and cause trouble (level change and jitter). This is called “Crosstalk”.

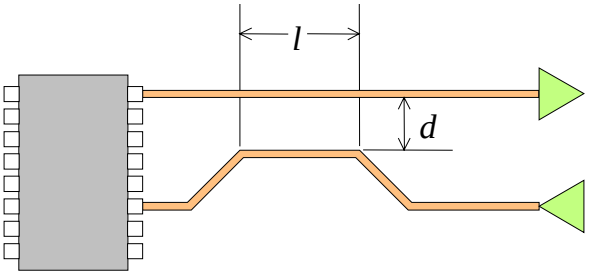


Figure 55 Signal Lines

To avoid the crosstalk in your test circuit, you must consider the following:

- For traces that carry high frequency signals (such as clock), do not draw these traces in parallel.
- (If possible) Use a coaxial cable to protect any sensitive signal from noise.
- Increase the distance between traces.
- Decrease the adjacent surfaces by bending the traces.
- Use a guard line between traces.

Troubleshooting Noise Problems

During test circuit development, you may encounter one or several of the following problems:

- A correctly specified filter does not cut the signal as required.
- A relay does not disconnect a signal completely.
- A weak signal shows exessive noise.
- A DC reference voltage has high frequency spikes.

Such problems are likely to be caused by poor isolation or crosstalk.

Consider the following measures:

- Change the position of components or cables. Separate input and output lines physically.
- Use coaxial cables to protect sensitive signals.
- Ensure that all ground connections are as short as possible.
- Increase the digital and analog ground planes.
- Add bypass capacitors.
- Use guard lines to shield voltage force/sense lines.
- Consider adding relays as shown below:

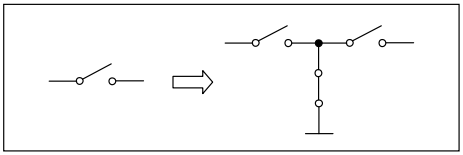


Figure 56 Troubleshooting DUT Board Problems

6

Device PowerSupply

This chapter provides you with information about the various Power Supplies available for the Agilent 93000 SOC Series Tester.

There are three types:

- *"General Purpose Power Supply (GPDPS)"* on page 136
- *"High Current Power Supply (HCDPS)"* on page 168
- *"High Voltage Power Supply (HVDPS)"* on page 181

The following sections describe these in detail.

General Purpose Power Supply (GPDPS)

This section provides you with information on:

GPDPS General Description

For normal applications, the Agilent 93000 SOC Series is equipped with the general purpose Device Power Supply GPDPS providing a voltage range from –8 to +8 V, for powering the DUT.

GPDPS Boards reside inside the testhead, each containing independent DPS channels with all grounds connected at the GPDPS main board (not cascadable). Each DPS channel can source and sink current at a programmed voltage.

Voltages and currents supplied can also be measured. For this purpose, four measurement ranges are provided.

To best adapt DPS channels to the appropriate test requirements you can also select between 4 different performance ranges that switch the internal gain of the DPS control loop.

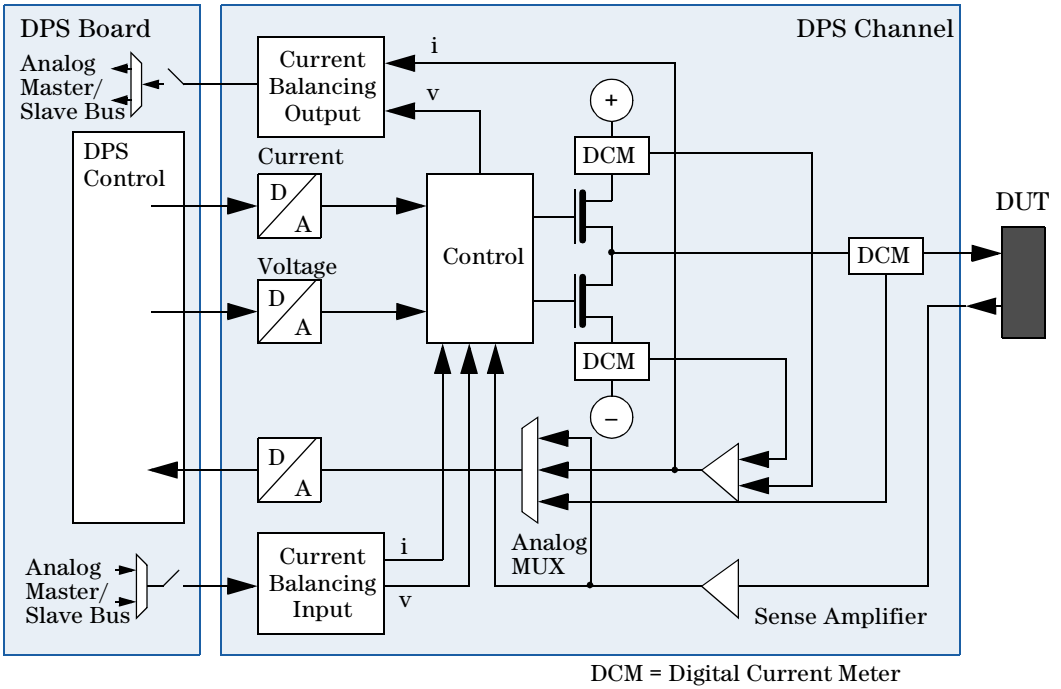


Figure 57 GPDPS Channel Block Diagram

Important features of the General Purpose Device Power Supplies are:

- Each DPS channel has two DACs for voltage setting. A trigger input (Vbump input) lets you switch between these two DACs.
- Each DPS channel is supplied with two current DACs - one to set a positive current limit (clamp) and one to set the negative current limit.
- Power up and hardware reset puts all four channels of a GPDPS board into HIZ mode.
- Each DPS channel can measure the voltages and currents supplied.

Maximum Number of Power Supplies

- **448** pin testhead: 16 slots, 1–4 GPDPS Boards (DPS1, DPS2, DPS3, DPS8) with 4 DPS Channels each
- **960** pin testhead: 32 slots, 1–8 GPDPS Boards (DPS1–DPS8) with 4 DPS Channels each

Switching DPS Voltages

Switching DPS voltages during test execution is possible using the digital Vbump feature (refer to *"Switching DPS Voltages (Vbump)"* on page 155)

Ganged GPDPS Channels

Parallel connections, in order to achieve a higher output current, are possible for up to 32 channels (max. 4 groupings). But note that no parallel connections with different supply types are possible (refer to *"Ganging GPDPS Channels"* on page 159)

GPDPS Specifications.

The following supply voltage/current range specifications apply for the General Purpose Device Power Supply:

Mode	Range	Resolution	Accuracy	Comments
Voltage force	–7...+7 V –8...+8 V	1 mV 1 mV	±5 mV ±0.1% ±5 mV ±0.1%	I_{max} = +8 A, –4 A I_{max} = ±4 A
Voltage measure	–8...+8 V	1 mV	±5 mV ±0.1%	
Current force (clamp)	–4 A, +8 A	1 mA	±20 mA ±0.5%	16 samples
Current measure	–8...+8 A –0.3...+0.3 A –10...+10 mA –100...+100 µA	1 mA 30 µA 1 µA 10 nA	±20 mA ±0.1% ±450 µA ±0.15% ±10 µA ±0.1% ±100 nA±0.1%	16 samples 16 samples C_{load} < 100 µF, 32 samples C_{load} < 1 µF, 500 samples

Table 26 General Purpose DPS: Voltage / Current Range Specifications

Voltage and Current Measurements

For current measurements, four ranges are available. In test functions that use the GPDPS as a measuring unit, autoranging is used to find the best current range.

The lowest current range provides the highest measurement accuracy. Note, that this measurement accuracy can only be guaranteed for a load capacitance less than 1µF and at least 500 samples. A load capacitance of 1 µF is only possible if the GPDPS operates within the performance range 1. In all other performance ranges the minimum capacitive load to ensure stable GPDPS operation is larger. See also *"Setting up Performance Ranges"* on page 141.

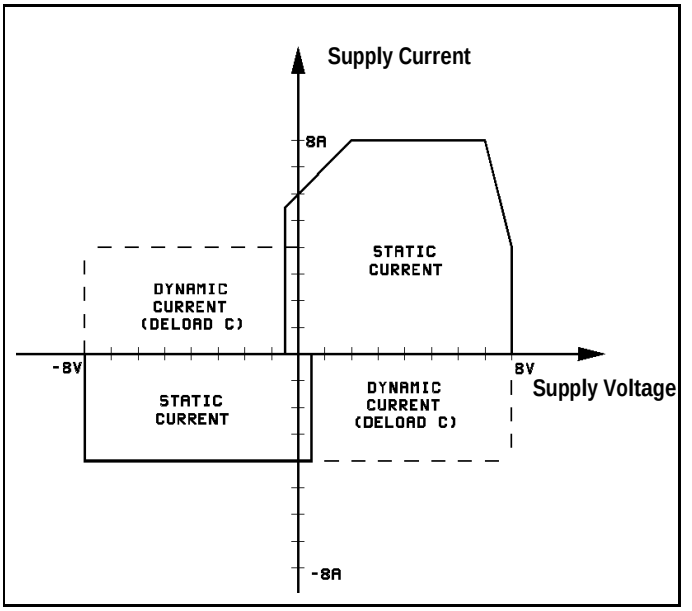


Figure 58 General Purpose Power Supply: Power Diagram

NOTE Current measurement ranges and performance ranges are completely independent of each other.

There is only a dependency with respect to the maximum achievable measurement accuracy. As mentioned above, this accuracy can only be achieved if the maximum capacitive load does not exceed 1µF. This is only possible when operating the GPDPS in the performance range 1, as the minimum capacitive load to ensure stable GPDPS operation is higher in all other performance ranges.

For more details on current measurements see *"Current and Voltage Measurements with DPS"* on page 164.

Setting up Performance Ranges

To fully exploit the benefits of the GPDPS design, which includes highest measurement accuracy for IDDQ current measurements and excellent regulation of current variations, performance ranges for the Agilent 93000 SOC Series General Purpose Device Power Supply have been introduced.

The subsequent sections explain the new concept in detail and lead you through the required setup steps.

What is a Performance Range?

The General Purpose Device Power Supply can be operated in four different performance ranges. Each performance range sets a different internal amplification of the GPDPS control loop. The performance range can be set independently for each GPDPS channel.

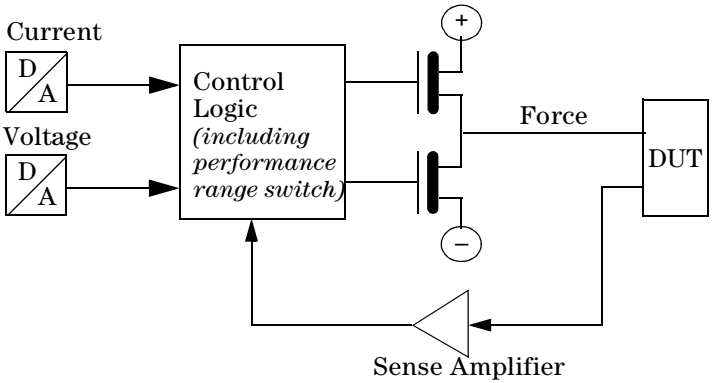


Figure 59 GPDPS Channel: Simplified Block Diagram

Figure 59 shows the simplified block diagram of a GPDPS channel. The control loop ensures that the actual programmed DPS voltage is applied to the DUT. Within the control logic, the open loop gain of the control loop can be changed by setting the appropriate performance range.

An essential component of the GPDPS is the load capacitor that needs to be added at the DPS pin. This load capacitor ensures that the GPDPS operation is stable under all load conditions. Its size depends on the performance range set.

NOTE You must not operate the GPDPS without an adequate load capacitor. The GPDPS will only provide stable operation with an adequate blocking capacitor.

The following performance ranges are available:

Range	Min. Cload (required for stable operation)
1	100 nF
2	4 µF
3	20 µF
4	100 µF
Range 1 max. current: 3 A DC, all other ranges 8 A DC	

Table 27 GPDPS Performance Ranges

In the column C_{load}, the load capacitance needed to ensure stable operation of the GPDPS in the respective performance range is specified. *Never* operate the GPDPS with *less* than the load capacitance specified in this table. You can, however, increase the load capacitance to achieve a higher voltage supply level stability.

Basically, ranges 2, 3 and 4 can all drive current swings up to 8A, current range 1 can drive current swings up to 3A. However, each performance range covers a specific current swing range best. Depending on your application needs (current swing of DUT, voltage supply stability needs), you need to find an appropriate combination of performance range and load capacitance. Read through the section *"Dynamic Load Performance Considerations"* on page 145 to find a suitable setup.

Why are Performance Ranges Useful?

Performance Ranges guarantee the best trade-off between measurement accuracy in iddq measurements and the capability of the GPDPS to drive a specific current swing.

In other words, performance ranges permit the characteristics of a GPDPS channel to be adjusted to suit a specific DUT.

Current swings up to 8A can be regulated with a single GPDPS channel operating in performance range 4.

The achievable measurement accuracy in performance range 1 is ±100nA±0.1% (minimum number of samples: 500) as long as the blocking capacitor does not exceed 1µF.

In general, the higher the performance range, the higher the load capacitance needed. For current measurements, the load capacitance should be as low as possible to reduce noise to a minimum and thus achieve highest possible measurement accuracy.

How to set up the Correct Performance Range

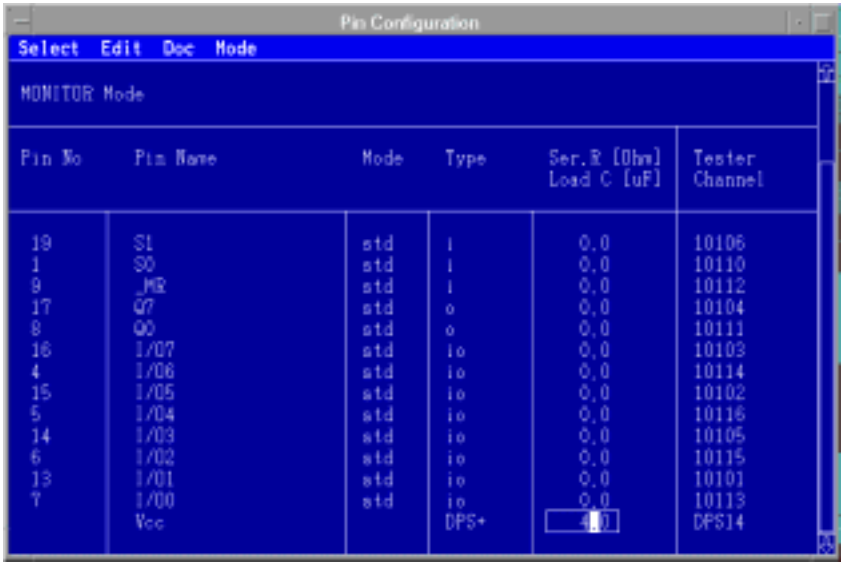
To set up the correct performance range proceed as follows:

1. Determine the maximum current step your DUT is likely to require.
2. Determine the appropriate performance range (see *"Dynamic Load Performance Considerations"* on page 145).
3. Ensure that the load capacitance at the DUT pin is not less than the load capacitance needed for stable operation (see *Table 27* on page 142).

4. Find out the maximum voltage ripple your DUT can tolerate. Dimension the load capacitance (C_{load}) accordingly.

   "Dynamic Load Performance Considerations" on page 145 helps you to find an adequate load capacitance.

5. Set the performance range by opening the Pin Configuration Editor window and type in the appropriate value of the load capacitance (load C) in the Ser.R [Ohm] Load C[υF] column against the V_{cc} Pin for the performance range you require. This is shown in the last line of the following figure.



   On the basis of this information, the GPDPS will automatically select the corresponding performance range according to the following schema:

   – Load C 0.1µF to < 4µF selects the performance range 1

- Load C 4µF to < 20µF selects the performance range 2
- Load C 20µF to < 100µF selects the performance range 3
- Load C ≥ 100µF selects the performance range 4

Note: It is also possible to set or change the performance range in your device setup with the firmware command PSCL:

PSCL *<performance range>, (<Pinlist>)*

<performance range> := 1, 2, 3, 4

Dynamic Load Performance Considerations

The sense line monitors the DPS voltage level and the control logic regulates the current so as to maintain the desired DPS voltage level.

The response time of the control loop to changes in the load conditions is small but not zero. To buffer the supply voltage level immediately after a change in the load conditions, a load capacitance is needed. This load capacitance ensures stable operation of the GPDPS control loop. It acts as a low pass filter, stabilizing the supply voltage.

The following parameters influence the dynamic performance of the GPDPS channel:

- performance range

  The higher the performance range, the higher the open loop gain of the GPDPS control loop. In a higher performance range the GPDPS can better react to higher current swings without introducing high supply voltage ripples. On the other hand, higher performance ranges require higher load capacitances.

- load capacitance

  Basically, each performance range requires a minimum load capacitance to ensure stable operation. Further increasing the load capacitance increases the low pass filter effect and smooths the supply voltage from large voltage ripples if load conditions change. Alternatively, high load capacitances slow down dynamic performance and introduce current noise into GPDPS current measurements. This is especially undesirable in low current measurements (standby or iddq currents).

The following parameters are of importance from an application point of view:

- maximum current swing

  A high current swing can occur during operation, if the DUT switches from the standard operational state to the quiescent state or vice versa. This is typically the current swing to be considered when selecting the performance range.

- stability of supply voltage range

  To guarantee an optimal supply for the DUT, the supply voltage must be stable within a certain voltage range. Minimum and maximum supply voltages are specified in the DUT's specification sheet. As a rule of thumb, to guarantee supply voltage stability, the load capacitance needs to be increased to decrease voltage ripple.

- measurement accuracy for low current measurements (iddq, standby)

  Any load capacitance introduces current noise in a current measurement. The impact on the measurement accuracy can be significant for very low current measurements. In general, to take full advantage of the high GPDPS current measurement accuracy, the load capacitance should not be larger than 1µF.

The following table helps you to find the appropriate performance range and capacitive load:

Range	Min. Cload	CDV<200mV	Current swing	CDV<200mV	Current swing
1	100nF	100 nF	60 mA	<4 µF	100 mA
2	4µF	4 µF	300 mA	<20 µF	400 mA
3	20µF	20 µF	1.0A	<100 µF	1.5 A
4	100µF	100 µF	3 A	3000 µF	8 A
Range 1 max. current: 3 A DC, all other ranges 8 A DC					

Table 28 GPDPS Performance Ranges and Characteristics (Voltage ripple ≤ 200 mV)

For each performance range, the minimum essential capacitive load (Min. C_{Load}) that is always required is shown together with two pairs of current swing values and their respective capacitive loads, dimensioned so that the supply voltage ripple will be less than 200mV for the respective current swing. These reference values help you find the appropriate load capacitances for the particular performance range and current swing of the DUT to keep the voltage ripple below 200mV.

Note that the current swings shown are maximum values within which the power supply ripple will not exceed 200mV. They do not, however, represent the only current swings permissible for the particular range. If, for example, your expected current swing is 150mA, although this could be handled by the performance range 1, you should preferably use the performance range 2 with 4µF to produce the lowest voltage ripple (in this case well below 200mV).

On this basis, performance range 1 is typically used for current swings up to 100mA (although current swings of up to 3A could be regulated with this performance range), performance range 2 typically for current swings in the

range of 100mA to 400mA, performance range 3 typically for swings in the range of 400mA to 1.5A and performance range 4 typically for swings in the range of 1.5Ato 8A.

The following figures show the relationships between the voltage supply ripple and the smoothing capacitance for various current swings in each performance range. They may be of assistance to help you to find the most appropriate performance range and tailor the load capacitance to reduce the voltage ripple to your particular needs. Ensure, however, that you adhere to the minimum capacitive requirement for the selected performance range as shown in the table *"GPDPS Performance Ranges"* on page 142.

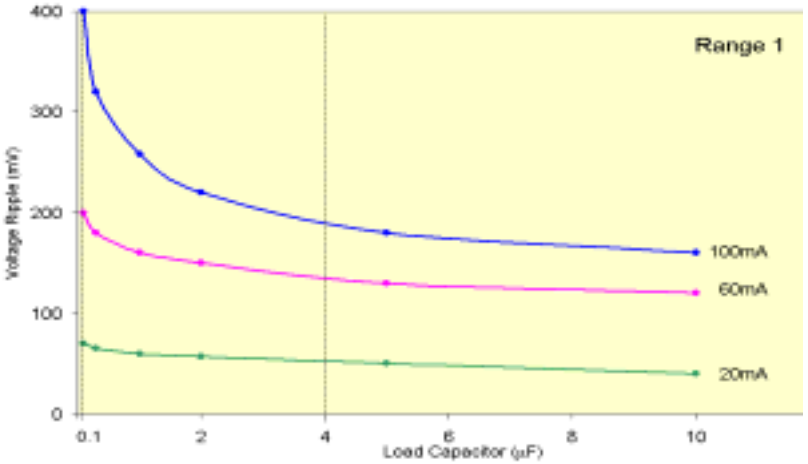


Figure 60 Relation Between Load Capacitance and Voltage Ripple - Range 1

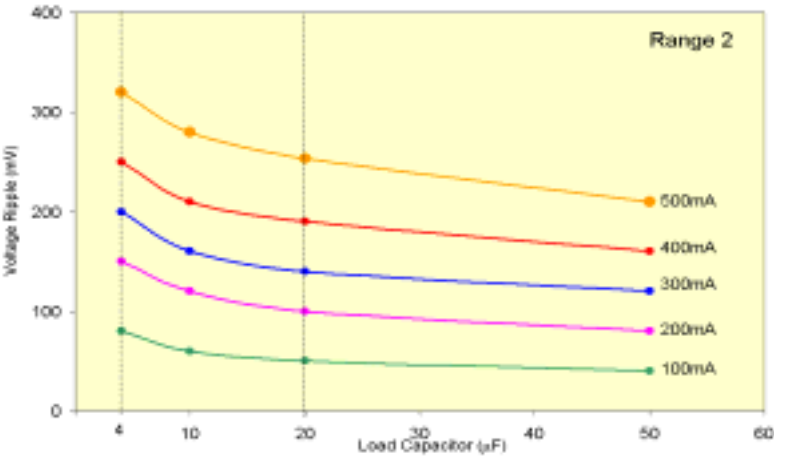


Figure 61 Relation Between Load Capacitance and Voltage Ripple - Range 2

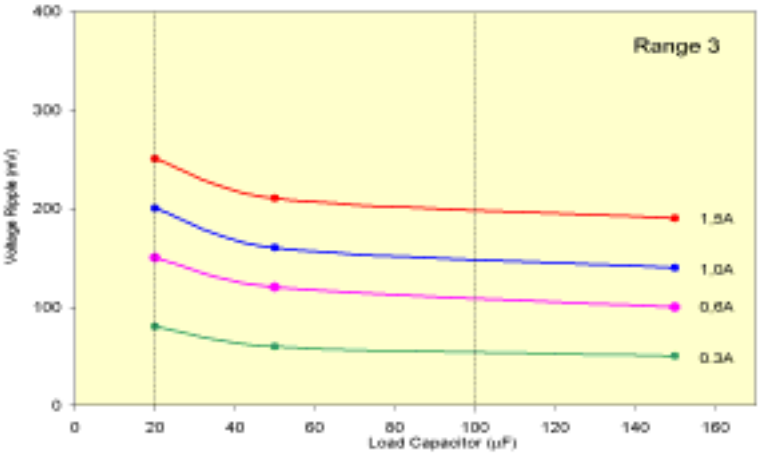


Figure 62 Relation Between Load Capacitance and Voltage Ripple - Range 3

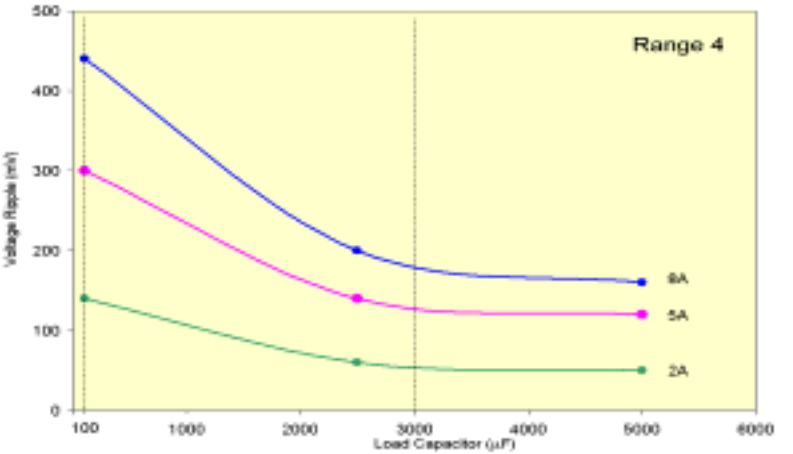


Figure 63 Relation Between Load Capacitance and Voltage Ripple - Range 4

Examples of Dynamic Load Performance

To illustrate the GPDPS characteristics, examples of measurement plots are illustrated in the following figures.

The measurement setup used is shown in *Figure 64*. One measurement for each performance range has been performed using a hand-wired loadboard. In performance ranges 1 and 2, low ESR (Equivalent Series Resistance) capacitors have been used and in performance ranges 3 and 4 through-hole electrolytic capacitors.

The current step response at the GPDPS pin has been measured for each performance range using an adequate current step and load capacitance.

In general you will observe that:

- the voltage ripple is less than 200mV in all performance ranges
- it takes less than 1ms to recover the original voltage supply level in all performance ranges

If you further increase the load capacitance, the initial voltage ripple will be reduced but voltage ringing may appear. See also the example *"Measurement in Performance Range 2 with High Load Capacitance"* on page 153.

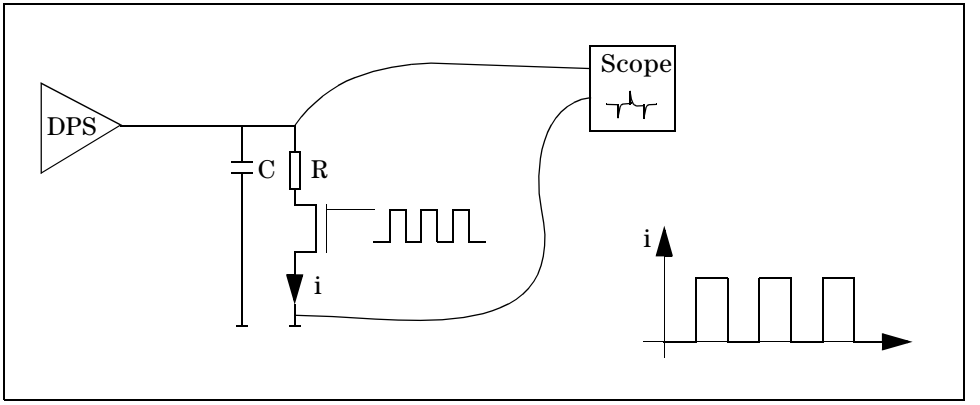
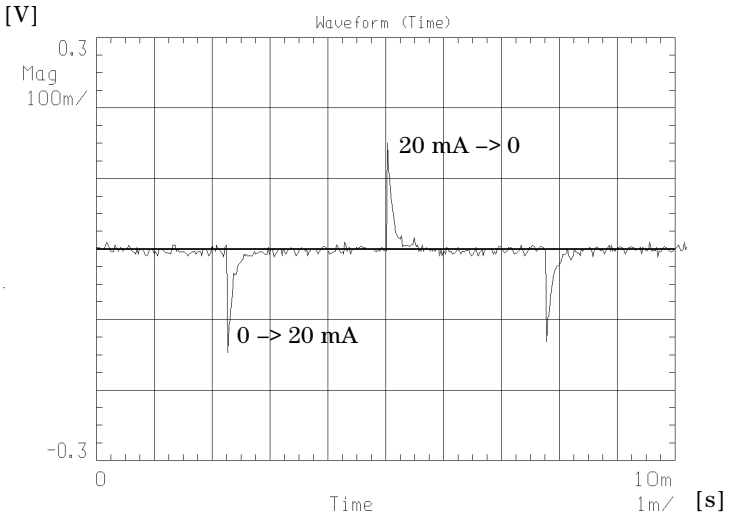


Figure 64 Measurement Block Diagram

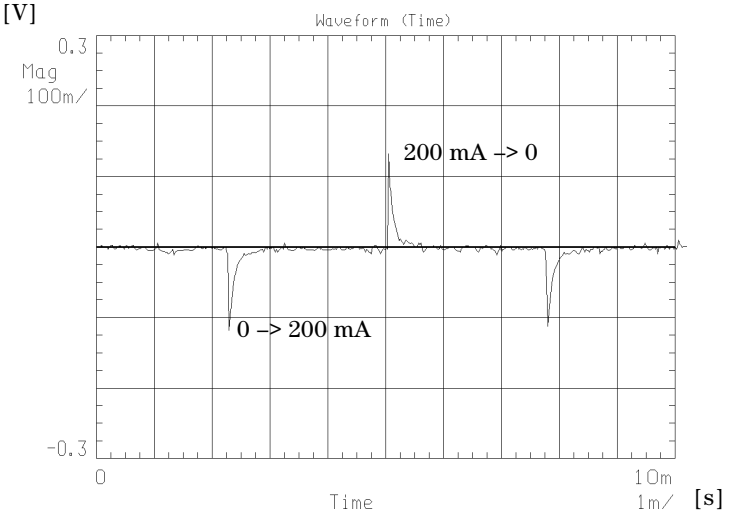
Measurement in Performance Range 1



U = 4.5 V
C = 100 nF
0 <–> 20 mA

Figure 65 Load regulation in performance range 1

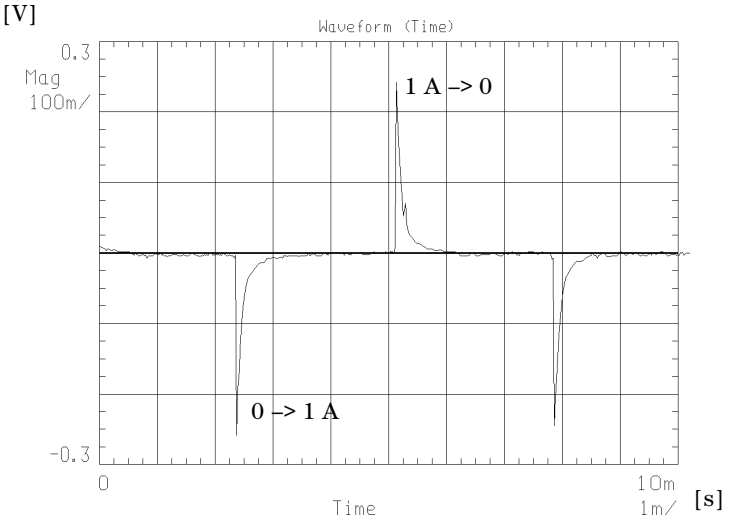
Measurement in Performance Range 2



U = 4.5 V
C = 4 µF
0 <–> 200 mA

Figure 66 Load regulation in performance range 2

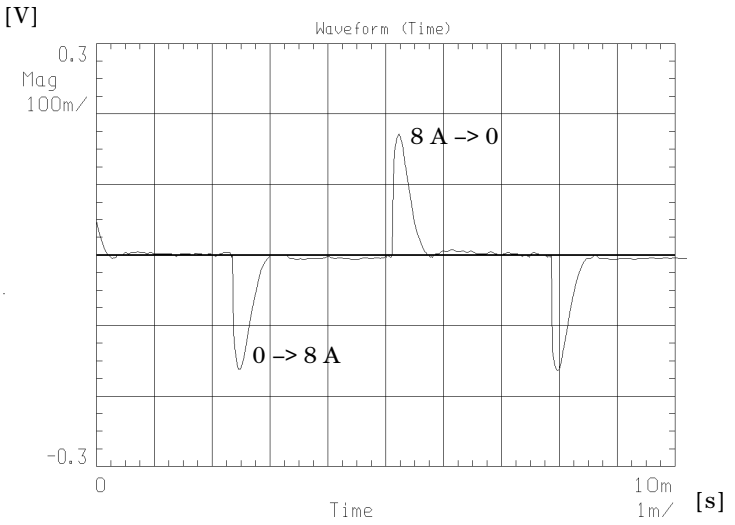
Measurement in Performance Range 3



U = 5 V
C = 20 µF
0 <–> 1 A

Figure 67 Load regulation in performance range 3

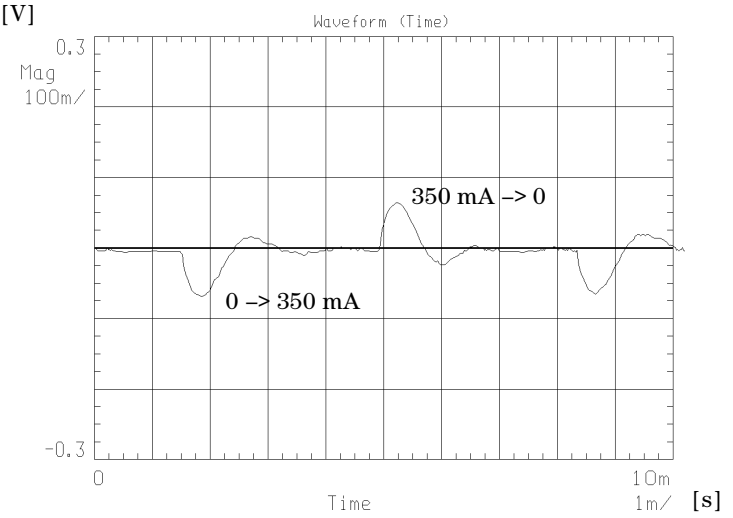
Measurement in Performance Range 4



U = 4.5 V
C = 3000 µF
0 <–> 8 A

Figure 68 Load regulation in performance range 4

Measurement in Performance Range 2 with High Load Capacitance



U = 8 V
C = 1000 µF
0 <–> 350 mA

Figure 69 C-overload performance in range 2

The effect of a high load capacitance in this performance range can clearly be seen:

- the voltage ripple is reduced
- ringing occurs
- recovery of the DPS voltage level takes longer

Decoupling Recommendations

Powering noise-sensitive DUTs requires noise filtering on a load board level. For this purpose, installation of bypass capacitors is necessary.

NOTE Do not confuse these bypass capacitors with the load capacitor needed to ensure stable operation of the GPDPS.

Radio Frequency Decoupling

Connect a small high-frequency decoupling capacitor as close as possible to each power pin of your DUT. The optimum value for this capacitor depends on your specific application, however, you can normally use a ceramic capacitor of 1 nF to 22 nF. Surface-mount capacitors provide the best results, because of their reduced lead inductance.

Filtering out GPDPS Related Noise

Due to the DC/DC converters which provide the GPDPS with power, the Device Power Supplies generate noise in the high-frequency range (basically 1 MHz and 200 kHz). You can filter out this noise by means of a ceramic bypass capacitor at the DUT.

Noise	Capacitance
< 30 mVpp	100 nF (min.)
< 20 mVpp	500 nF
< 10 mVpp	1 µF (max.)

Table 29 Bypass Capacitance to Filter Out GPDPS Related Noise

For noise-sensitive applications, we recommend a capacitance of 1 µF. Larger values will reduce measurement accuracy.

Switching DPS Voltages (Vbump)

Switching of DPS voltages is, for example, needed in data retention tests.

You can switch between two programmed power supply voltages without stopping the test using the digital V_{bump} feature. This feature allows you to program a change in the power supply voltage during device operation.

The advantages are:

- the supply voltage can be switched during execution of the pattern
- the measurement can be synchronized with the vector pattern
- all GPDPS channels can be triggered at one time

NOTE Each GPDPS channel provides two voltage DACs. The V_{bump} functionality lets you switch between the two voltage DACs on the DPS channel.

One Vbump trigger input is provided per DPS board. The trigger signal triggers Vbump simultaneously on all 4 DPS channels of the GPDPS board. However, you can set a mask in the level setup window to trigger only a subset of the 4 channels if you wish.

If the trigger signal goes from 0V to 5V, Vbump is triggered and the DPS switches to the second voltage. Because the voltage switching requires a small settling time, the DUT pins are disconnected (BREAK) during this period. This is illustrated in the *Figure 70* below which also shows the trigger paths.

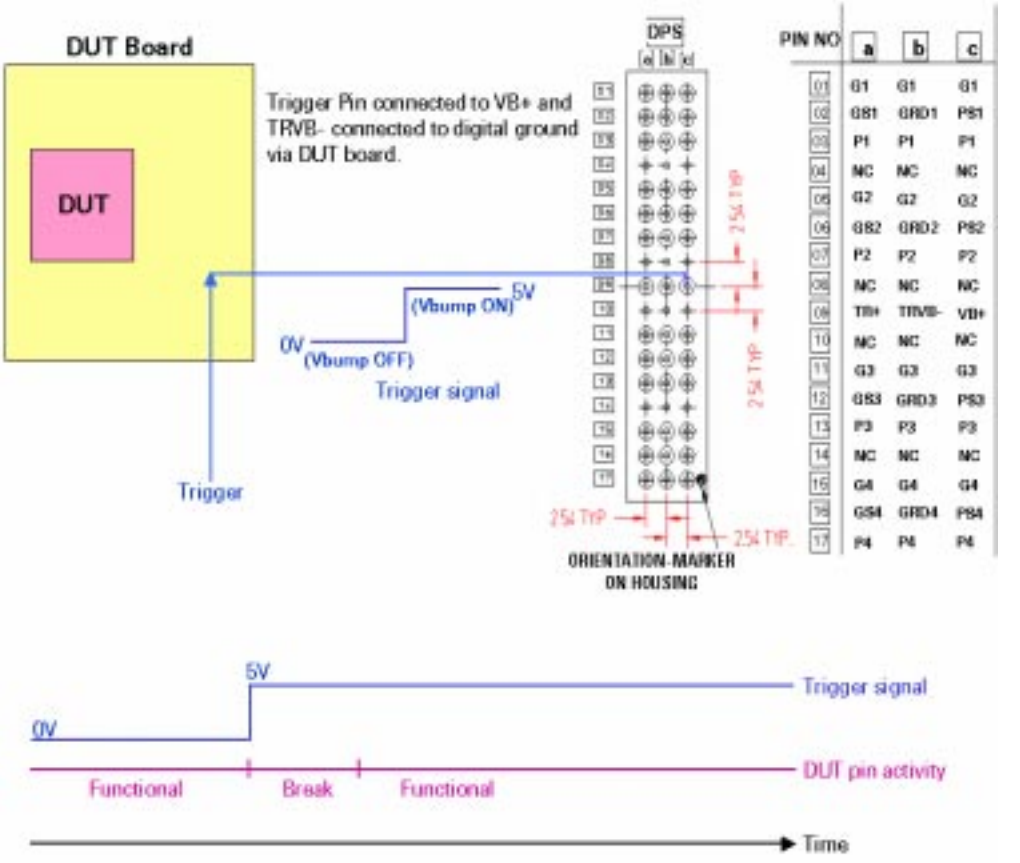
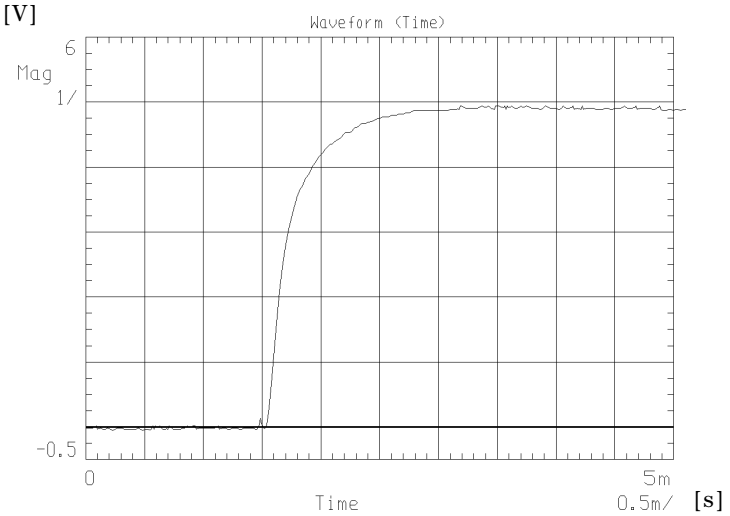


Figure 70 Vbump Trigger Paths and Function

Voltage Settling Times

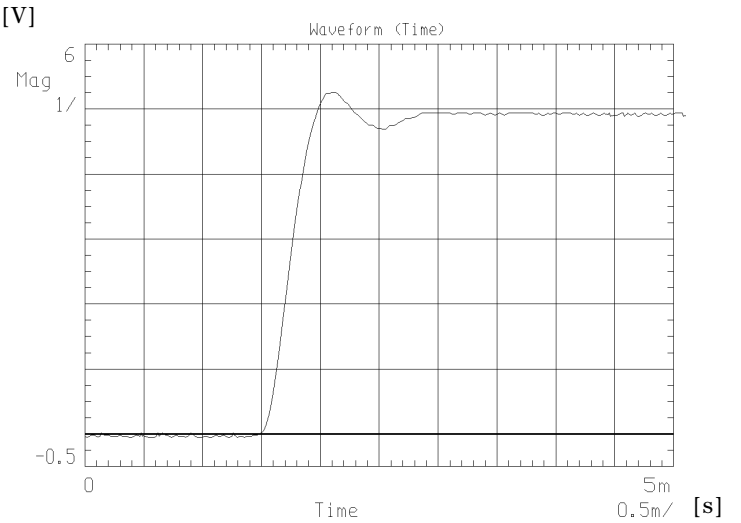
The voltage settling time is defined by an internal 1 kHz RC-low pass filter. This low pass filter is needed to limit overshoots during voltage steps. The plots shown below illustrate that voltage settling is easily predictable in most situations (*Figure 71* on page 157).

NOTE There is no significant difference in the voltage settling behaviour between: connect operation, reprogramming of voltage, or the V_{bump} function.



0 –> 5 V
Performance
Range 1

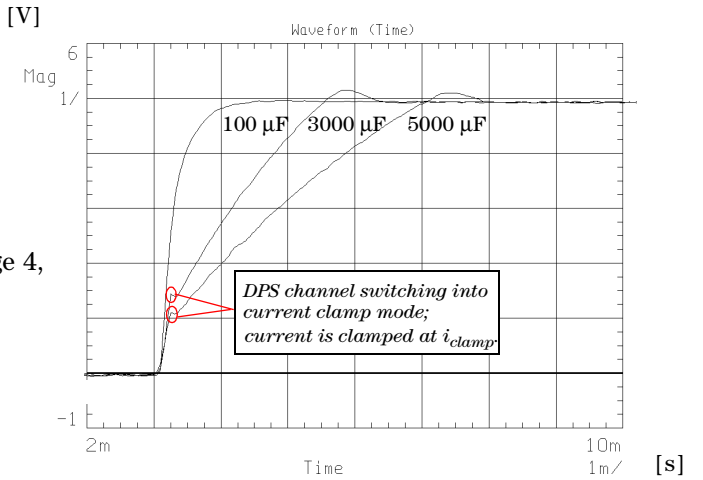
Figure 71 Voltage settling, load capacitance 100nF



0 –> 5 V
Performance
Range 1

Figure 72 Voltage settling, load capacitance 100µF

This plot illustrates what happens if the load capacitance is too high. Transient oscillations will occur.



0 –> 5 V,
performance range 4,
C_{load} = 100 µF,
C_{load} = 3000 µF,
C_{load} = 5000 µF
iclamp = 8 A
R_{load} = 1 Ω

Figure 73 Voltage step, high load (quadrant 1)

If the load capacitor is too high the DPS channel switches into current clamp mode. The current clamp mode limits the maximum DPS current. As can be seen, this behavior results in a significantly increased voltage rise time.

Ganging GPDPS Channels

In order to achieve a higher output current, you can operate multiple GPDPS channels in parallel, known as the **Ganged Mode**. This mode is useful e.g. for large CPUs and modules.

Ganging is defined as combining multiple GPDPS channels for the purpose of providing a current higher than that obtainable from a single GPDPS channel.

Consider n DPS channels ganged together. The result will be the current and voltage shown below.

$$I_{\text{ganged}} = n \cdot I_{\text{DPS}} \qquad V_{\text{ganged}} = V_{\text{DPS}}$$

Max. current: up to 8 A per General Purpose DPS channel, up to 16 A per General Purpose DPS board.

NOTE It is not possible to operate DPS channels in series to provide a higher output voltage.

How to Gang Supplies

As mentioned on *page 138*, you can gang up to 16 (for the 448 pin testhead) or 32 (for the 960 pin testhead) General Purpose DPS channels in 4 groups (each group consisting of a master channel and slaves where necessary).

Note that although each master can support up to 15 slaves, the allocation of masters and slaves must be made such, that the total number of 16 or 32 channels is not exceeded.

The channels of one ganged group have to be in sequence (e.g. DPS11, 12, 13, 14, 21 etc.).

Note that it is not possible to gang different types of power supplies together.

For details on cable assembly on the DUT board refer to *"Routing DPS Lines"* on page 163.

Setting up Ganged GPDPS Channels

Basically, ganged GPDPS channels can be set up in the Pin Configuration window. Ganging GPDPS channels is done by assigning the same pin ID to these channels. Combine a consecutive number of "slave" channels to a "master" channel. The numbering of the slave channels has to follow sequentially from the number of the master channel. The first channel in this consecutive row of GPDPS channels is automatically set as the master channel. For details, see the *Test Setup* manual.

On the firmware level, the commands DFPS and DDSL are used in this conjunction.

DFPS <master_channel>,<polarity>,<(pin)>

DDSL <number_of_slave_channels>,<(pin)>

In the following example, slave channels 12, 13 and 14 are ganged with master channel 11 for pin Vee:

DFPS 11,POS,(Vee)

DDSL 3,(Vee)

NOTE Multiply the value of the load capacitor with the number of ganged channels.

Correctly Positioning Ganged GPDPS Connections

All ganged channels must be allocated sequential numbers. For example, if you want to configure three GPDPS channels for a supply pin, and the first channel is DPS11, the following channels must have channel numbers DPS12 and DPS13.

All Power (Force+) and Ground (Force–) pins and all Sense pins must be wired on the DUT board according to the *Figure 74* on page 161. To avoid introducing an unwanted potential difference between the DUT pin and the ganged connections, make the connection as close as possible to the supply pin.

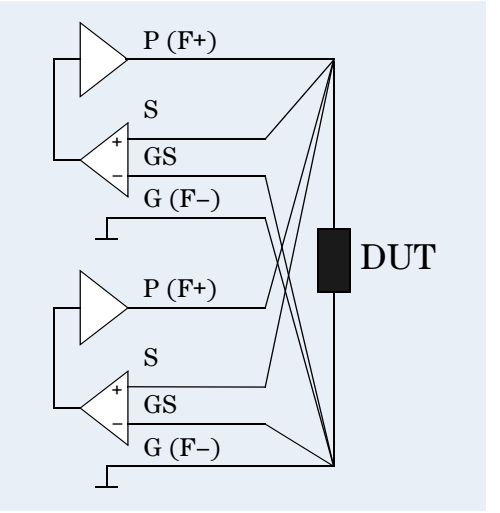


Figure 74 Ganged DPS Connections

Disconnecting the DPS

A connected DPS forces the programmed power supply voltage (FW command PSLV). The current is limited to the connect current limit.

If the supply reaches the current limit, the voltage at the DUT is decreased. In this case, warnings are displayed in the Report Window.

A disconnected DPS can be in one of two modes:

- High-Impedance Mode
- Low-Impedance Mode

High-Impedance Mode

In high-impedance mode (HIZ), the DPS is switched to high-z mode.

Impedance = 10 kΩ (Revision A) and 1 MΩ (later revisions)

In order to activate the high-impedance mode, set the impedance in the PSLV firmware command to “HIZ”.

NOTE At power-up of the test system all DPS channels are set to HIZ mode.

Low-Impedance Mode

In low-impedance mode (LOZ), the DPS is active, forcing 0 V (General Purpose DPS). This allows capacitors to discharge after disconnecting the DPS channel.

In order to activate the low-impedance mode, set the impedance in the PSLV firmware command to “LOZ”.

Routing DPS Lines

Ensure that Power and Ground lines are laid out one directly above the other.
Wire width = 3 A/mm^2.

Sense lines must be positioned close together and parallel to each other to avoid induction of interference. Furthermore, Sense/Force connections must be positioned as close as possible to the DUT. Failure to observe this rule will cause you to include the potential difference developed across the track between the DUT pin and the sense point in your measurement.

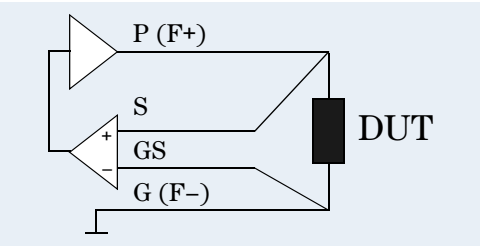


Figure 75 DPS Connections

You can check the DPS connectivity with the DPS Connectivity Test (refer to the *Standard Test Function Reference*, Part No. E7050-91012).

Current and Voltage Measurements with DPS

Device Operation Sequence

The figure below shows a typical device operation sequence.

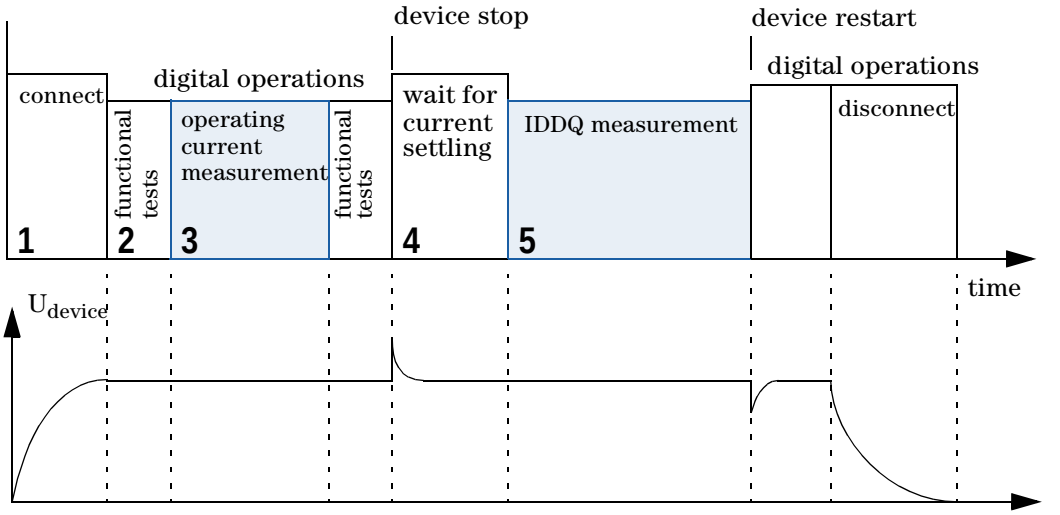


Figure 76 Device Operation Sequence

1. Connect: Please note the transient time. The current measurement will be incorrect, if measured too quickly after the connect phase. The transient time depends on the test environment (load capacitance, device etc.). Be cautious if initial current measurement is carried out < ~ 5 ms after connect.
2. Functional tests: No measurements during functional tests.
3. Operating current measurement: Normally, digital operations are required within the device. The current should be constant to ease sampling.

4. Device stop: Wait time due to transient time of the voltage controller and the resulting balancing currents in the load capacitor.

There is no difference in the execution time for a firmware command or test function, whether the test executes for pass/fail results or for results by value.

Due to autoranging, the measurement time depends heavily on the value to be measured.

NOTE If you require the highest measurement accuracy (in current measure range 1, accuracy ±100nA±0.1%), the maximum load capacitance must not exceed 1µF. This means that, if the DPS is operating in a higher performance range, you will need to switch to performance range 1 to be able to reduce the capacitive load to 1µF.

The measurement operation sequences (3 and 5 in *Figure 76* on page 164) is expanded in the figure below.

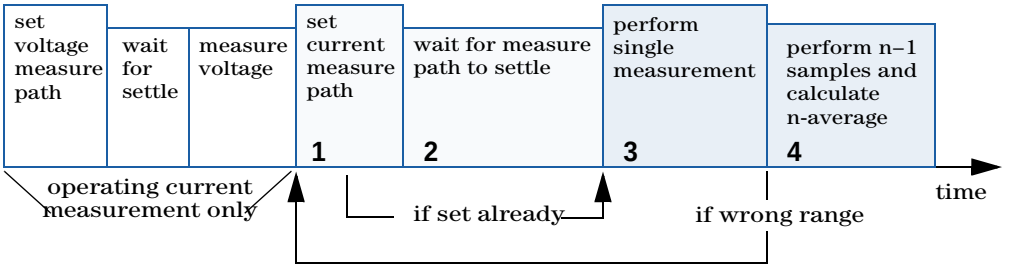


Figure 77 Measurement Operation Sequence

1. Before the current measurement, the measurement path will be set (operating current: 300 mA–average, IDDQ: 100 µA–average).
2. If the measurement path is switched by the hardware, a wait time is required.

Range	Wait time (GP-DPS)
Voltage	0.5 ms
10 A	0.07 ms
300 mA	0.1 ms
10 mA	0.1 ms
100 µA	5 ms

Table 30 Wait time required for measurement path to settle

3. In order to select the subsequent measurement path (autoranging), a single measurement is used.
4. After the measurement path has settled, the remaining measurements are performed.

Measurement Range	Samples
Voltage	1
10 A	16
300 mA	16
10 mA	32
100 µA	64 (+ user samples)

Table 31 Number of samples depending on range

Measurement time per sample:
~ 30 µs min. (ADC + data transfer) +
~ 10...50 µs depending on computer type and load

NOTE The time required for a single measurement varies, because a multitasking system is employed which is interruptible. Thus, the values given are statistical.

NOTE If the disconnect pin list in the IDDQ test function is *not* empty, it will require additional time to open the I/O pin relays.

Sample IDDQ Current Settling Time

The table below shows the settling time required for static IDDQ current measurements (sample IDDQ only). The load step appearing when halting the clock, has to be regulated by the DPS. It results in a current flowing through the measurement shunts into the DUT bypass capacitor. The minimum settling time depends on the load and test situation and should be evaluated on a case by case basis.

Capacitor	Current Settling Time
100 nF	~ 3 ... 6 ms
4 µF	~ 5 ... 8 ms
20 µF	~ 5 ... 8 ms
100 µF	~ 5 ... 8 ms

Table 32 Sample IDDQ Current Settling Time

In related test functions, the wait times are automatically set (there is no need to specify them explicitly).

High Current Power Supply (HCDPS)

This section provides you with information on:

HCDPS General Description

The High Current Power Supply is required as a power source for devices, often requiring only low voltages but drawing high currents or having large current swings, such as the following:

- High-end Microprocessors
- Multichip Modules

Each HCDPS provides 100A and two HCDPS can be ganged together to provide up to 200A. The modules reside inside the testhead. Note, however, that the HCDPS board only contains one supply (channel) and not four as is the case with the General Purpose and High Voltage power supplies. Furthermore, in contrary to the GPDPS and HVDPS, the HCDPS does not have performance ranges.

As with the General Purpose and High Voltage DPS, the High Current DPS can also measure currents and voltages (see *"Current and Voltage Measurement"* on page 178).

Connection to DUT Board

The HCDPS is connected to the DUT Board with a special high current, low impedance connecting cable.

The cable ends in a pogoblock, consisting of 4 special power pins (Force +) and 4 power ground pins (Force -), capable of carrying 100 ampere in total.

In addition, the pogoblock contains eight more pogopins for the following signalling purposes:

- sense +
- sense - (ground sense)
- +5V dut
- safety_line
- S_GND
- Trig
- Vbump
- current_monitor

Block Diagram

The following figure shows, in principal, the layout of the HCDPS

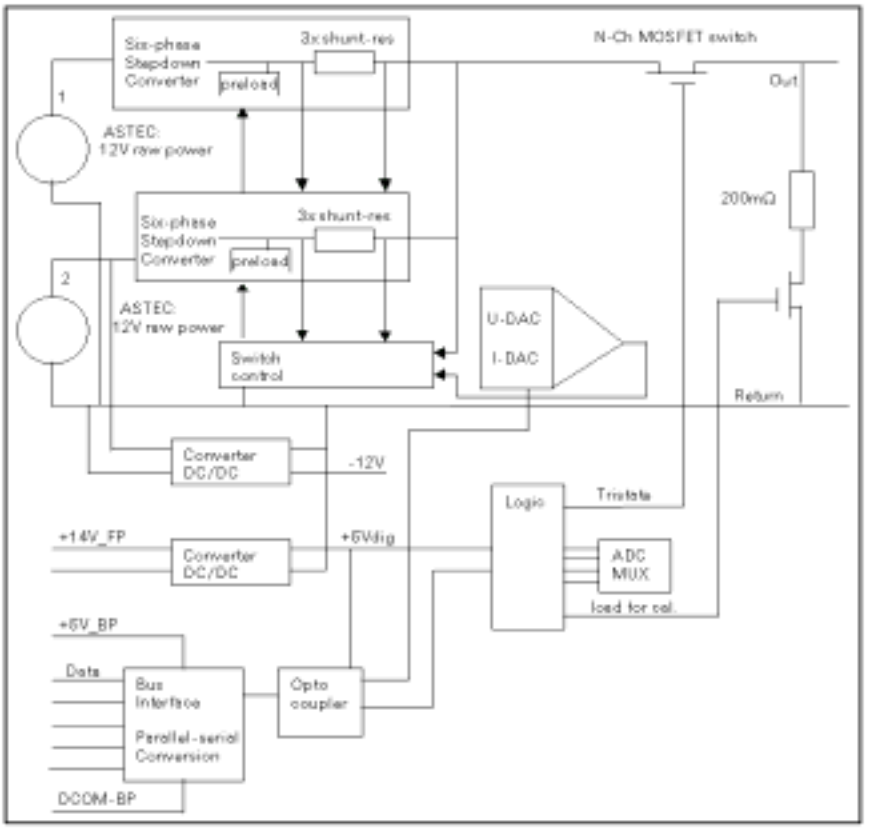


Figure 78 High Current DPS Block Diagram

The main sections of the HCDPS consist of

1. The BUS interface

   This is basically the same as the BUS interface for the General Purpose DPS.

2. The multiphase stepdown converter

   This converter steps down two raw +12V supplies to the required output level.

   It consists of an array of 2, 6 phase step-down converters, each phase shifted 30 degrees to each other. Because of this multiphase technology, ripple and the size of the circuit is minimized and speed is enhanced. Each pair of switches has its own 4-wire series resistor to measure current. The single measurements are summed up to the total output current which can be used for current limiting and current monitoring. This converter delivers its power via a tristate switch directly to the output. Because such a buck converter is not able to sink currents, pre-loads are included. These pre-loads are 2.2 Ohm for output voltages >3V and 0.7 Ohm for output voltages < 3V.

3. Safety circuits

   The following safety precautions are included in the HCDPS:

   a. Isolation

      The 100A-low impedance cable to the DUT Board includes, among others, three signal pins: S_GND, +5Vdut and safety_line. All three pins are isolated from the HCDPS via optocouplers and are floating.

   b. Shut Down

      The +5Vdut line must have +5V (relative to S_GND) applied to it for the HCDPS to operate. The safety_line is connected to the +5Vdut line via an internal pull-up resistor. The HCDPS monitors this line: If high, the HCDPS operates correctly, if pulled down, the HCDPS will be switched to tristate. This line is bidirectional: When the HCDPS detects an internal failure, it will pull down this line. This line also allows you to synchronously shut down different supplies in the event of a failure.

c. Over-temperature Protection

It is possible to add a heat or smoke sensor to the DUT-Board in such a way, that, in the event of an emergency, the safety_line will be pulled down resulting in a shutdown of all HCDPS units simultaneously.

d. Over-voltage Protection.

Here, there are three levels of protection:

I) Programmable protection: This is set with the Firmware command PSOP as described on *page 178*. This protection can be made active (at 4 different over-voltages) or inactive. The default is inactive (over-voltage protection off). The protection switches the HCDPS to tristate in order to protect the DUT.

II) If the Voltage at the output of the HCDPS is more than about 1.8V above the programmed value, three diodes in series between the output and the regulator begin to conduct and regulate voltage down to that level.

III) If the Voltage at the output of the HCDPS rises to more than 4.8V, a crowbar circuit short-circuits the 12V supply voltage of the HCDPS itself.

Note: I) is the standard protection for tests, and is slow enough not to be triggered under normal operating conditions, the protection offered by **II**) and **III**) is normally only necessary if severe problems occur inside the HCDPS.

e. Over-current Protection

There are two modes to be considered here:

I) Constant current mode: When the current limit is reached, the HCDPS operates as a constant current source. **Note:** Constant current mode is not possible in ganged mode.

II) Clamp mode: When the current limit is reached, the DPS switches to tristate.

For these modes, three different delay times (2ms, 6ms, and 8ms) can be programmed using the firmware command **HSCM** (for details of this command see the section, *"Firmware Commands for the HCDPS"* on page 178 or the *Command Reference* manual).

Note: When the DPS switches to tristate because of having reached current limit, it does not pull down the safety line

4. Balancing Circuits.

The 12 phase stepdown converter is organized in 6 pairs, phase-shifted by 180° to each other. Each pair has its own shunt resistor to measure its output current. All 6 current measurements are summed up to a mean value. Regulators compare the mean value with each of the 6 single currents and balance them to be equal. If the current of one stage rises so much that the balancing is never possible, a failure signal is generated which:

a. Switches the HCDPS to tristate.

b. Creates a flag to be read by the software.

c. Switches also all HCPS to tristate which are connected to the same safety_line.

5. Diagnostic Circuits

   As with the General Purpose and High Voltage power supplies, the HCDPS contains additional circuits for diagnostic purposes.

   The following diagnostic facilities are provided:

   – Detection of failure of ASTEC-raw power.

   – Detection of overcurrent and overvoltage.

   – Detection of the state of safety-lines at the DUT-Board.

   – For measuring the impedance i.e. the voltage drop on the power lines, the ADC is able to measure between **sense+** and **sense-** as well as between power out of the HCDPS board and the return path of the HCDPS board.

   – Check of Master/Slave connections.

   Diagnostics of the HCDPS board consists mainly of 2 independent tests, as in the case of the General Purpose (GPDPS) and High Voltage (HVDPS) Power Supplies:

   a. Standard HCDPS diagnostics.

   b. At-speed HCDPS diagnostics.

   The maximum test current for the standard diagnostics is 8A, so for a full current test (100A), the *at-speed* diagnostics must be performed.

   Due to the special pogo block assembly for the HCDPS, a special loadboard is required to run the *at-speed*

diagnostics. This means, that you cannot run any other tests while performing the *at-speed* test.

The HCDPS *atspeed* loadboard is configurable and can be adapted to each testhead configuration for HCDPS boards at various positions.

To permit the HCDPS to be tested at maximum current, each HCDPS pin is short-circuited. This test can only be carried out in current mode.

DPS Connectivity and DPS Status checks are described in the *Standard Test Function Reference* manual, Part No. E7050-91012.

6. Trigger Circuit

   As with the General Purpose and High Voltage DPS, the High Current DPS can be triggered from a DUT board with a 5V signal to start automatic measurements.

   The DPS is able to make any ADC measurement either using the internally triggered mode with a firmware command or externally triggered. In the external trigger mode, a FIFO circuit with a size of 64k can collect up to 32k of measuring data. There is one such trigger input per device which floats and uses S_GND as a reference.

HCDPS Specifications

Type	Value	Resolution	Accuracy
Voltage force	0.3...2.5V (100 A_{max}) 2.5...4V (50 A_{max})	1mV	±5mV
Voltage measure	0V...4V	1mV	±5mV
Current clamp	+1...100A	100mA	for I≤10A: ±(200mA+0.5% of value) for I>10A: ±(200mA+2% of value)
Current measure	±100A	10mA	for 0-100A: ±(100mA+0.4% of value) negative currents without calibration

Table 33 High Current DPS: Voltage / Current Range Specifications

Note that in contrast to the General Purpose and High Voltage DPS, there is only one voltage and current range.

When looking at minimum currents to be measured, please take into account:

- The base accuracy of the GDPS is about 0.25% of full scale. This represents 20mA for 8A. Compared to this, the accuracy of the HCDPS is 200mA for 100A.
- A static load with negative currents is not possible, hence, no such calibration can be performed.
- The voltage is programmable down to 0V for testing the protection diodes of the DUT (Continuity Test).
- The current measurements in ganged mode sum up the individual values of 200mA accuracy for each HCDPS module to a total value of 400mA.

HCDPS Decoupling Recommendations

This is described under *"Decoupling Recommendations"* on page 154.

HCDPS Switching Voltages (Vbump)

This is described in *"Switching DPS Voltages (Vbump)"* on page 155.

Note, however, that the HCDPS board only contains one supply (channel) and not four as is the case with the General Purpose and High Voltage Power Supplies.

Ganging HCDPS Boards

Normally a maximum of two boards can be ganged together to generate up to 200A. The basic procedure for doing this is described in the section covering the General Purpose Power Supply (GPDPS) on *page 159*. However, you must consider:

- The High Current DPS contains only one channel per board and not four, in contrast to the General Purpose and High Voltage DPS.
- Normally, a maximum of only two HCDPS boards (=channels) can be ganged together

Note that it is not possible to gang different types of power supplies together.

Disconnecting the HCDPS

This is the same as described on *page 162* except that an HCDPS disconnected in the low impedance mode, forces a small positive voltage (mV) not 0V as with the GPDPS.

Routing HCDPS Lines

The principles described in the section *"Routing DPS Lines"* on page 163 apply to the HCDPS also.

Current and Voltage Measurement

As with the General Purpose and High Voltage DPS, the High Current DPS can be triggered with a +5V signal (see *"Trigger Circuit"* on page 175) to cause it to commence with measurements of voltages and/or currents.

As the HCDPS only has only one range, it measures all currents in the high current range.

For measurements of small currents, the HCDPS can be switched to tristate to allow more accurate measurements to be made using an SPMU or GPDPS, connected in parallel (measurements using the GPDPS are described in the section, *"Current and Voltage Measurements with DPS"* on page 164).

A current monitor output is fed to the DUT Board by one of the eight signal pogo pins. The output is 3V/100A. Source impedance of this output is 10k Ohm. The reference for this output is ground sense (**sense** -).

Voltage measurements can also be carried out using the HCDPS.

Firmware Commands for the HCDPS

For the High Current DPS there are two new firmware commands as follows:

1. PSOP and PSOP?

   Description:

   The **PSOP** (Power Supply Overvoltage Protection) command specifies the overvoltage levels, at which a High Current DPS channel disconnects. Overvoltage

disconnect is a hardware functionality which is only available with the High Current DPS.

If this command is executed for the General Purpose DPS or High Voltage DPS, it will have no effect.

The **PSOP?** query returns the last programmed value.

Syntax:

PSOP <code>,{(pinlist)}

PSOP? {(pinlist)}
returns
PSOP <code>,{(pinlist)}

Parameters:

<code>
0 Overvoltage protection (disconnect) disabled.
1 Overvoltage disconnect at U>Uset+0.2V.
2 Overvoltage disconnect at U>Uset+0.4V.
3 Overvoltage disconnect at U>Uset+0.6V.
4 Overvoltage disconnect at U>Uset+0.8V.

2. HSCM and HSCM?

Description:

The **HSCM** (High Current Clamp Mode) command is similar to the **PSCM** command which sets the clamp mode for the General Purpose and High Voltage Power Supply channels.

The **HSCM** command has additional parameters for determining the delay time for switching off the power supply.

The **HSCM?** query returns the last programmed value.

Syntax:

HSCM {mode}

HSCM? {mode}
returns
HSCM {mode}

Parameters:

mode	This parameter specifies the DPS clamp mode and can take the values:	
	LIMIT	The output current is limited to the programmed current value.
	OFF	The affected DPS channel is switched off if overcurrent occurs. Other power supply channels remain in operation.
	DELAYED_1	The affected DPS channel is switched off after 2 ms if overcurrent occurs. Other power supply channels remain in operation.
	DELAYED_2	The affected DPS channel is switched off after 6 ms if overcurrent occurs. Other power supply channels remain in operation.
	DELAYED_3	The affected DPS channel is switched off after 8 ms if overcurrent occurs. Other power supply channels remain in operation.

High Voltage Power Supply (HVDPS)

This section provides you with information on:

For further details refer to the following sections of the General Purpose DPST:

HVDPS General Description

The High Voltage Power Supply is basically the same as the General Purpose Power Supply but with the following differences:

- The supply voltage is from 0.5V to 22V
- The *maximum* current is 1A

As with the General Purpose DPS, four channels (power supply modules) per board are provided and can be ganging, as described in the section *"How to Gang Supplies"* on page 159.

As with the General Purpose DPS, the High Voltage DPS is also operated in one of four performance ranges and a minimum load capacitor per range, as described in *Table 27* on page 142, is required for stable operation. See

also the section *"Setting up Performance Ranges"* on page 141 for more details, but note that although the General Purpose DPS can deliver currents of up to 8A, the High Voltage DPS can only deliver currents up to a maximum of 1A so that mention of currents above 1A are irrelevant for the High Voltage DPS.

HVDPS Specifications

The following supply voltage/current range specifications apply for the High Voltage Device Power Supply

Operation	Range	Resolution	Accuracy	Comments
Voltage force	0.5...22 V	2 mV	±10 mV ±0.1%	I_{max} = 1 A
Voltage measure	0.5...22 V	2 mV	±10 mV ±0.1%	
Current force (clamp)	1 A	1 mA	±20 mA ±0.5%	16 samples
Current measure	1 A 0.3 A 10 mA 100 µA	1 mA 30 µA 1 µA 10 nA	±20 mA ±0.1% ±300 µA ±0.15% ±10 µA ±0.1% ±100 nA ±0.1%	16 samples 16 samples C_{load} < 100 µF, 32 samples C_{load} < 1 µF, 500 samples

Table 34 High Voltage DPS: Voltage / Current Range Specifications

7

Analog Modules

Testing of mixed-signal devices requires analog resources for applying highly accurate analog signals to devices and capturing analog signals output from devices. Further, the analog resources are required to operate with digital signals synchronously.

The following kinds of analog modules are available for Agilent 93000 SOC Series testers:

- Arbitrary Waveform Generators (AWG)
- Waveform Digitizers (WD)
- Sampler
- Time Interval Analyzer (TIA)

This chapter describes the functionality, key specifications, and theory of operation for each analog module:

Also, this chapter describes the synchronization between the analog modules and digital signals:

Waveform Generators

There are three types of AWGs available as follows:

- **High Resolution AWG** (1 MSample/s 18-bit)
  — Code name: **WGA**
- **High Speed AWG** (128 MSample/s 12-bit)
  — Code name: **WGB**
- **Ultra High Speed AWG** (2.6 GSample/s 8-bit)
  — Code name: **WGC**

AWG Overview

The arbitrary waveform generator (AWG) can source sine waves, pulse waves, ramp waves, pseudo-random noise, and various other waveforms to DUTs. The AWG uses waveform data that is stored in the waveform memory to generate analog waveforms.

You create arbitrary waveform data with the software interface, Mixed-Signal Tool. The waveform segments that you create in the tool are the fundamental units of waveform data. The output order of waveform segments is controlled by the sequence program in the internal sequencer. You can create an AWG sequence program with the software interface, Analog Setup Tool. The waveform data is downloaded into the waveform memory, and the sequence program is downloaded into the sequencer.

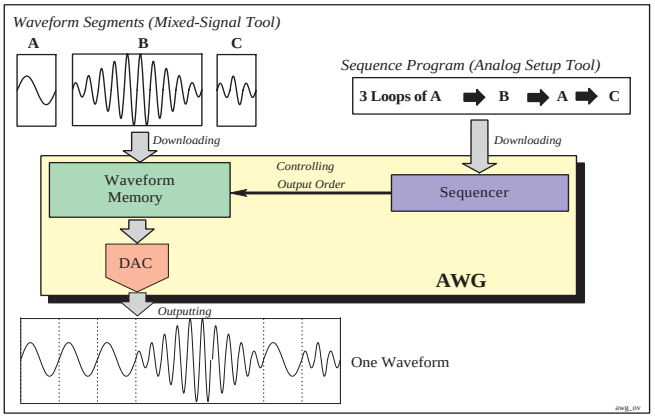


Figure 79 Analog Waveform Generation

The AWGs start waveform generation by entering the external triggers. Generally, a digital channel is used for each AWG as the external trigger source. A trigger signal must be supplied at the SYNC CLK pin. For more information of the synchronization trigger, see *"Synchronization Trigger"* on page 248.

The ultra high speed AWG can also output a digital signal that is synchronized with waveform data. This is called the marker function, and it outputs from the marker pin. The marker data is also created in the Mixed-Signal Tool.
You can use this marker output such as a trigger signal for monitoring the waveform during debugging.

The following tables show the key specifications of the AWGs.

Specification	Value
Pin counts per module	8 single-ended (4 parallel test) or 4 differential (2 parallel test)
Resolution	18-bit
Sampling rate	8 ksps to 1.024 Msps
Waveform memory	4 M
Max. sinewave frequency	250 kHz
Output mode	Single-ended, Differential
Output range	6 Vpp @600 ohm load (0 to 63 dB attenuation with 0.01 dB resolution)
DC offset range	±5 V @600 ohm load
Output impedance	50 ohm
Filter	Through, 1.3 kHz, 13 kHz, 130 kHz, 300 kHz
Waveform segment - Min. length	 6
Sequencing - Number of steps - Max. loop count - Max. nesting level - Output level @halt - Functions	 256 steps/block (32 blocks reloadable) 256 8 Keep last level - Halt when current waveform done - Continue next waveform - Counted loop of one/multiple waveforms - Infinit loop of one/multiple waveforms

Table 35 High Resolution AWG Key Specifications

Specification	Value
Pin counts per module	8 single-ended (4 parallel test) or 4 differential (2 parallet test)
Resolution	12-bit
Sampling rate	8 ksps to 128 Msps
Waveform memory	2 M
Max. sinewave frequency	32 MHz
Output mode	Single-ended, Differential
Output range	2.5 Vpp @50 ohm load (0 to 63 dB attenuation with 0.01 dB resolution)
DC offset range	±2.5 V @50 ohm load to GND 0 V to 5 V @50 ohm load to external termination voltage (2.5 V)
Output impedance	50 ohm
Filter	Through, 1.3 MHz, 6.1 MHz (Video), 13 MHz, 41.6 MHz
Waveform segment - Min. length - Number of data	 24 8 x *N* (*N*: integer)
Sequencing - Number of steps - Max. loop count - Max. nesting level - Output level @halt - Functions	 256 steps/block (32 blocks reloadable) 256 8 Keep last level - Halt when current waveform done - Continue next waveform - Counted loop of one/multiple waveforms - Infinit loop of one/multiple waveforms

Table 36 High Speed AWG Key Specifications

Specification	Value
Pin counts per module	8 single-ended (2 parallel test) or 4 differential (2 parallel test)
Resolution	8-bit
Sampling rate	50 ksps to 2.6 Gsps
Waveform memory	8 M
Max. sinewave frequency	400 MHz (Normal mode) 800 MHz (Direct mode)
Output mode	Differential pair
Output range	2 Vpp@50 ohm (Normal mode) (20 mVpp to 2.0 Vpp with 1 mV resolution) 1 Vpp@50 ohm (Direct mode) (20 mVpp to 1.0 Vpp with 1 mV resolution)
DC offset range	±1.0 V (Normal mode only)
Output impedance	50 ohm
Filter	Through, 20 MHz, 50 MHz, 100 MHz, 200 MHz
Waveform segment - Min. length - Number of data	 512 8 x *N* (*N*: integer)
Sequencing - Number of steps - Max. loop count - Output level @halt - Functions	 8000 65536 Keep last level - Halt when current waveform done - Continue next waveform - Counted loop of one waveform - Infinit loop of one waveform

Table 37 Ultra High Speed AWG Key Specifications

Theory of Operation for High Resolution and High Speed AWGs

This section describes the theory of operation for AWGs. The following is the block diagram of the high resolution AWG and high speed AWG.

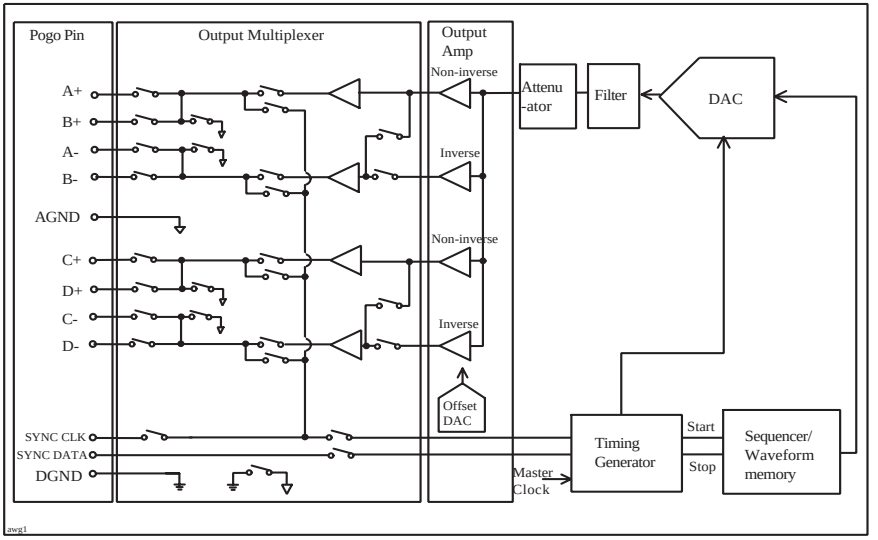


Figure 80 High Speed AWG and High Resolution AWG Block Diagram

All the components of the high resolution AWG and high speed AWG are installed in the testhead. The AWG consists of the following blocks.

- Output Multiplexer
- Output Amplifier
- Attenuator
- Low Pass Filter
- Digital-to-Analog Converter
- Timing Generator
- Sequencer and Waveform Memory

Output Multiplexer

The output multiplexer can make the following connections:

- Output routes
- DC routes
- Loop back routes

Output Routes

To output a single-ended signal or a pair of differential signals from the desired pogo pins, the output multiplexer makes the routes between the output amplifier and the desired pogo pins. The following figure shows possible routes for outputting a single-end signal.

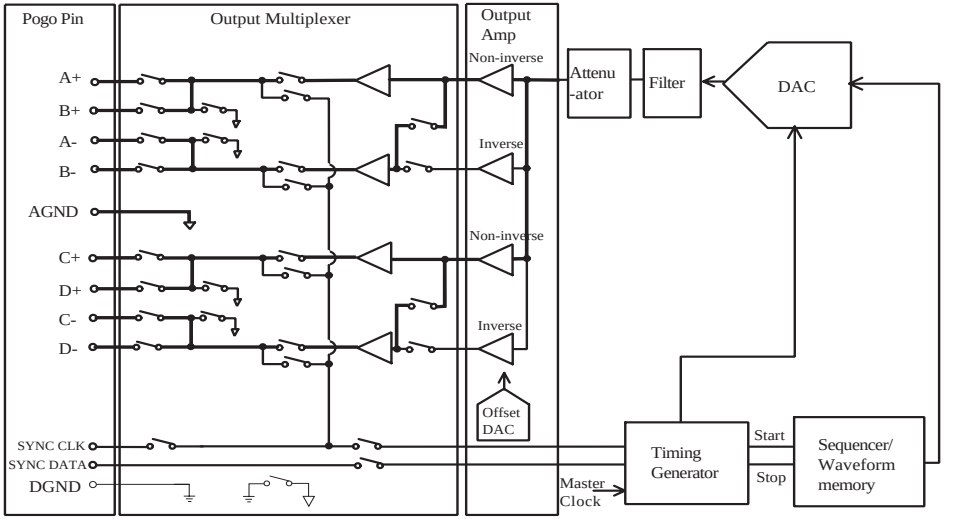


Figure 81 Output Routes (Single-ended)

The following figure shows possible routes for outputting a pair of differential signals.

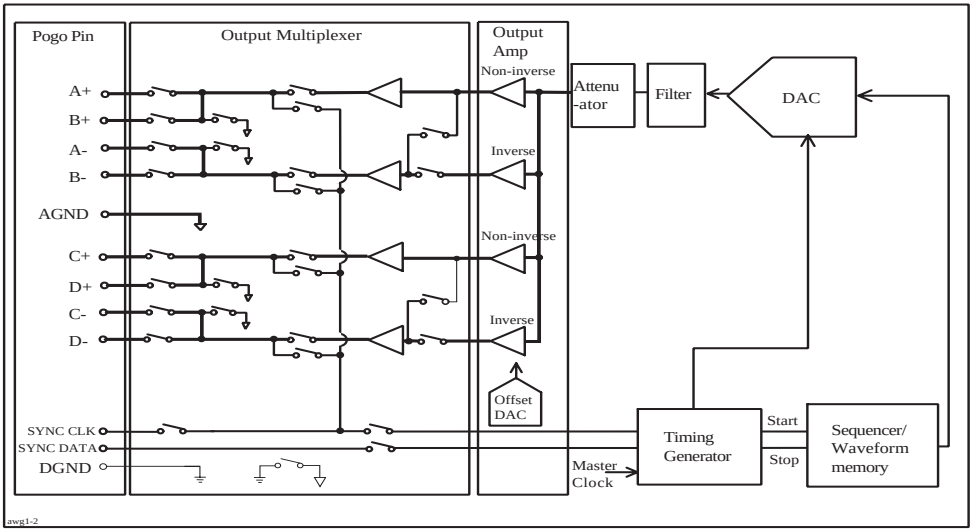


Figure 82 Output Routes (Differential)

A single-ended signal or a pair of differential signals can be output from multiple pogo pins at the same time. However, there are restrictions for the combination of the pogo pins. Because each pair of adjacent pogo pins, A+ and B+, A- and B-, C+ and D+, and C- and D- shares the same output amplifier, these pairs cannot be used at the same time. The following table summarizes the restrictions.

Mode	Possible Pogo Pin Combinations
Single-ended	All or some of following combinations: A+ or B+, A- or B-, C+ or D+, C- or D-
Differential	All or some of following combinations: Pair of A+/A- or B+/B-, Pair of C+/C- or D+/D-
Mix of single-ended and differential	Following two cases: (a) Single-ended A+ or B+, and/or A- or B-, AND differential pair of C+/C- or D+/D- (b) Single-ended C+ or D+, and/or C- or D-, AND differential pair of A+/A- or B+/B-

Table 38 Possible Pogo Pin Combinations

DC Routes

The output multiplexer can make the route between a pogo pin and the SYNC CLK pin. This enables DC measurement by using a Pin PMU on a digital channel connected with the SYNC CLK pin. Hence, if you wire a digital channel with the SYNC CLK pin on the DUT board, you can perform DC measurement at the DUT pin connected to the AWG by using a Pin PMU. The following figure shows the possible routes between the pogo pins and SYNC CLK pin, which are represented with bold lines. When the DC route is made, the output amplifier is disconnected from any pogo pins.

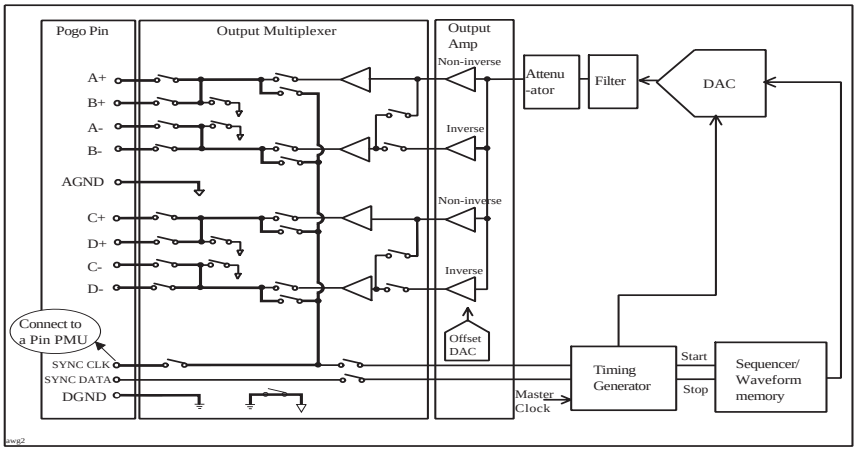


Figure 83 DC Routes

Loop Back Routes

The output multiplexer can make the loop back route between A+ and B+, between A- and B-, between C+ and D+, and between C- and D-. When a loop back route is made, it is disconnected from other routes. Hence, you can make multiple loop back routes, or also make a loop back route and another route (output route or DC route) using other pins at the same time. In the following figure, the possible loop back routes are represented with bold lines.

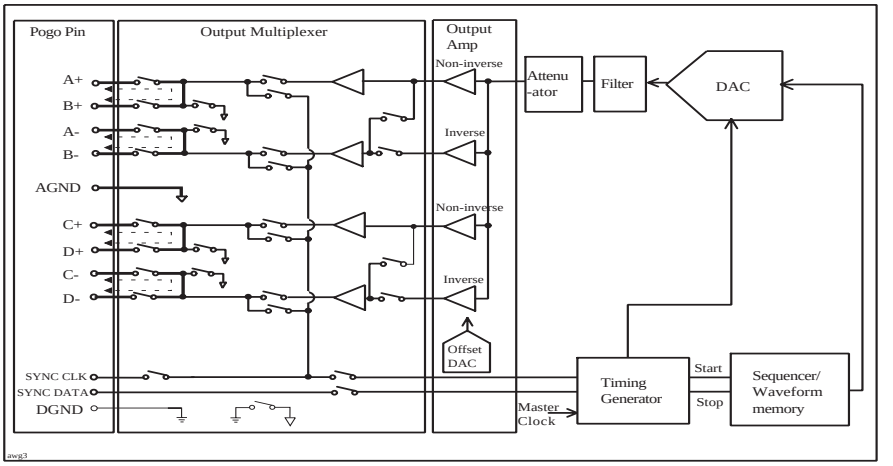


Figure 84 Loop Back Routes

The loop back route is designed so that the line impedance becomes 50 ohm exactly. As a result, the bandwidth of the loop back route extends up to 150 MHz (typical value) for the high resolution AWG, and 190 MHz (typical value) for the high speed AWG. So, by using the loop back route, you can make the route that has better performance than using additional user relays on the DUT board.

Output Amplifier

The output amplifier can distribute a single-ended signal transferred from the attenuator to the differential signals. The output amplifier can also add the DC offset voltage to the signals.

For the high speed AWG only, the output amplifier can drive within 2.5 V to 5.0 V (DC+AC output level) into 50 ohm termination to the external termination voltage that is equal or greater than 2.5 V. The termination voltage can be supplied by the other DC resource such as DPS.

Attenuator

The attenuator adjusts the amplitude of the signal generated by the digital-to-analog converter.

Filter

The filter is a low pass filter for smoothing the waveforms. This filter removes harmonics from the signal. There are several filters with different cut-off frequencies.

Digital-to-Analog Converter

The digital-to-analog converter (DAC) converts the digital waveform data transferred the waveform memory to the analog signal, according to the output sequence from the sequencer. The DAC converts the digital data to the analog signal according to the conversion clock provided by the timing generator.

Timing Generator

The master clock and trigger signal are input to the timing generator. After receiving the trigger signal, the timing generator starts to generate the conversion clock by dividing the master clock and feeds the conversion clock to the DAC. The timing generator also sends the start signal to the sequencer. The timing generator stops to generate the conversion clock when the sequencer is halted.

The timing generator contains the delay counter and delay vernier. By using them, the timing generator controls the delay time from when the trigger signal arrives at the trigger input pin to when waveform generation starts at the pogo pin.

Sequencer and Waveform Memory

The sequencer controls the output sequence of the waveform data stored in the waveform memory. The output sequence of the waveform data is specified in the sequence program that is contained in the sequence memory. The following information can be specified in the sequence program.

- Waveform memory area to output waveform signal.
- Sequence instruction. The following operations can be specified.
  - No operation (NOP instruction)

    After the waveform data specified in the current sequence program line is processed, the sequencer proceeds to the next line.
  - Halt after waveform (HALT instruction)

    After the waveform data in the current sequence program line is processed, the sequencer stops and waits for the next trigger.
  - Repeat waveform (RPT/RPTI instructions)

    The waveform data on the current sequence program line is repeated the specified number of times (RPT) or infinitely (RPTI).
  - Loop waveform (LOOP/LOOPI instructions)

    The waveform data on the multiple sequence program lines is repeated the specified number of times (LOOP) or infinitely (LOOPI). The start point of the loop is the sequence address specified by a parameter of the instruction.
    Further, the waveform data on the current sequence program line can be also repeated the specified number of times in the loop.

Theory of Operation for Ultra High Speed AWG

This section describes the theory of operation for the ultra high speed AWG. The following is the block diagram of the ultra high speed AWG.

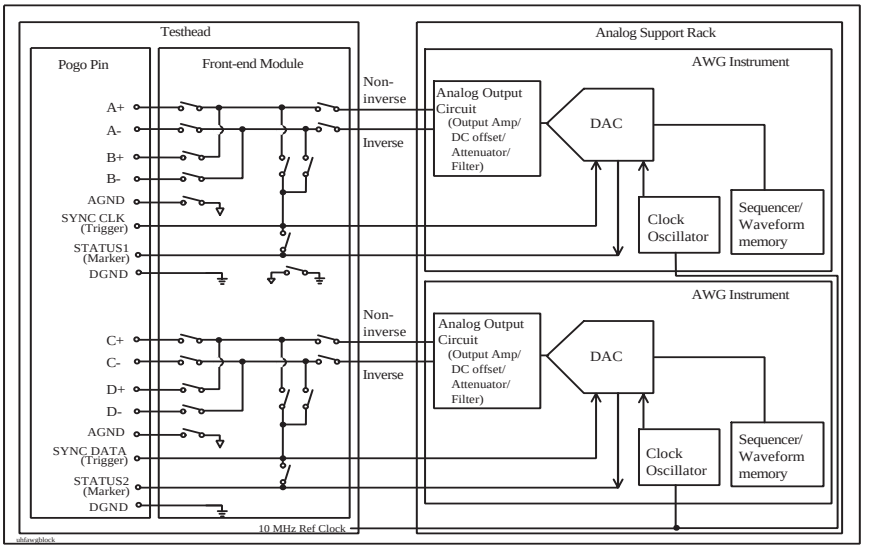


Figure 85 Ultra High Speed AWG Block Diagram

The ultra high speed AWG consists of the following blocks.

- Front-end Module in the testhead
- AWG instrument in the analog support rack

The following sections describe the functions of each block.

Front-end Module

The front-end module is installed in the testhead. One front-end module supports up to two AWG instruments installed in the analog support rack. *However, in the standard configuration, one front-end module supports only*

one AWG instrument shown as the upper block in the above figure. For one AWG instrument, the front-end module has four signal output pins, one trigger input pin, and one marker output pin.

The front-end module makes the following connections.

- Output routes
- DC routes
- Loop back routes

Output Routes

To output a single-ended signal or a pair of differential signals, the front-end module makes the route between the desired pogo pins and the AWG instrument outputs.

To output a single-ended signal, A+ or B+ can be used for channel 1. For channel 2, C+ or D+ can be used. In the following figure, the routes to output a single-ended signal are shown with bold lines.

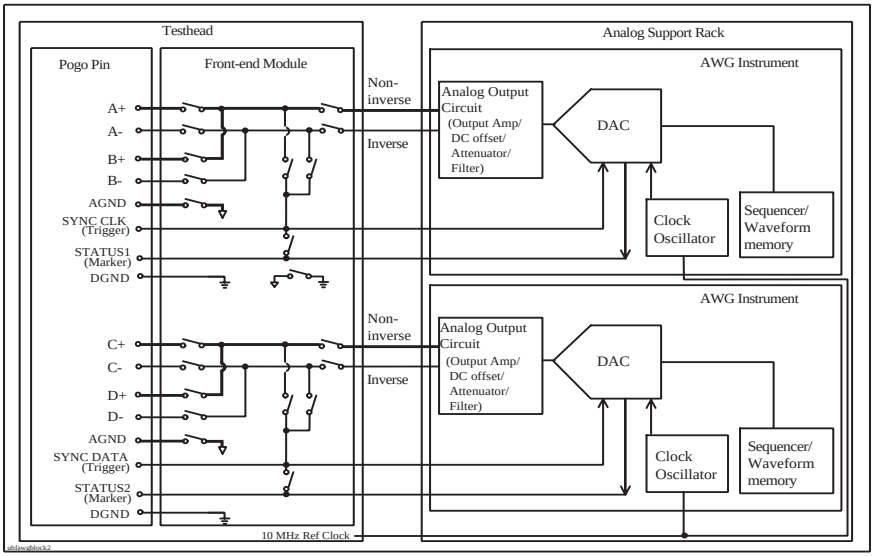


Figure 86 Output Routes (Single-ended)

To output a pair of differential signals, A+ and A-, or B+ and B- can be used for channel 1. For channel 2, C+ and C-, or D+ and D- can be used. In the following figure, the routes to output a pair of differential signals are shown with bold lines.

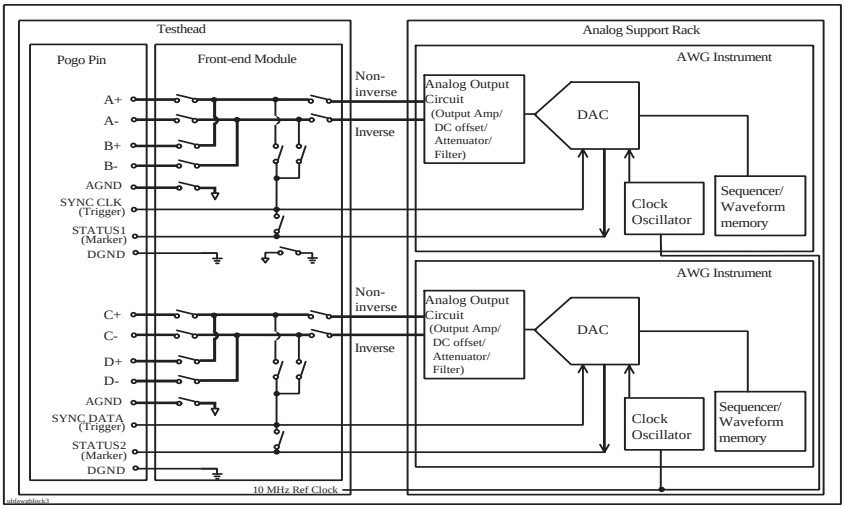


Figure 87 Output Routes (Differential)

DC Routes

The front-end module can make the route between a pogo pin (including the marker pin) and the trigger input pin. The trigger input pin is the SYNC CLK pin for channel 1 or the SYNC DATA pin for channel 2. This enables DC measurement by using a Pin PMU on a digital channel connected with the trigger input pin. Hence, if you wire a digital channel with the trigger input pin on the DUT board, you can perform DC measurement at the DUT pin connected to AWG by using a Pin PMU. The following figure shows the possible routes between the pogo pins and the trigger input pin, which are represented with bold lines. When the DC route is made, the AWG instrument is disconnected from any pogo pins.

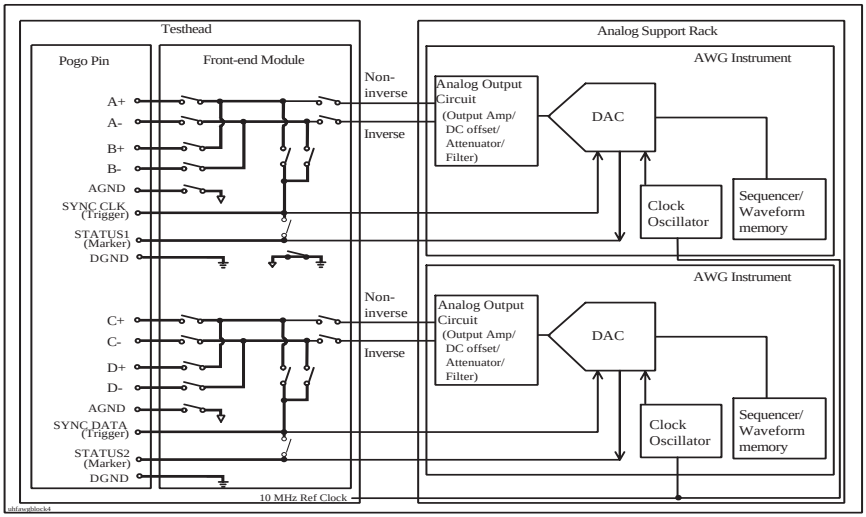


Figure 88 DC Routes

Loop Back Routes

The front-end module can make the loop back route between A+ and B+ and between A- and B- for channel 1. For channel 2, it can make the loop back route between C+ and D+ and between C- and D-. When a loop back route is made, the loop back route is disconnected from other routes. Hence, you can make multiple loop back routes, or make a loop back route and another route (output route or DC route) using other pins at the same time. In the following figure, the possible loop back routes are represented with bold lines.

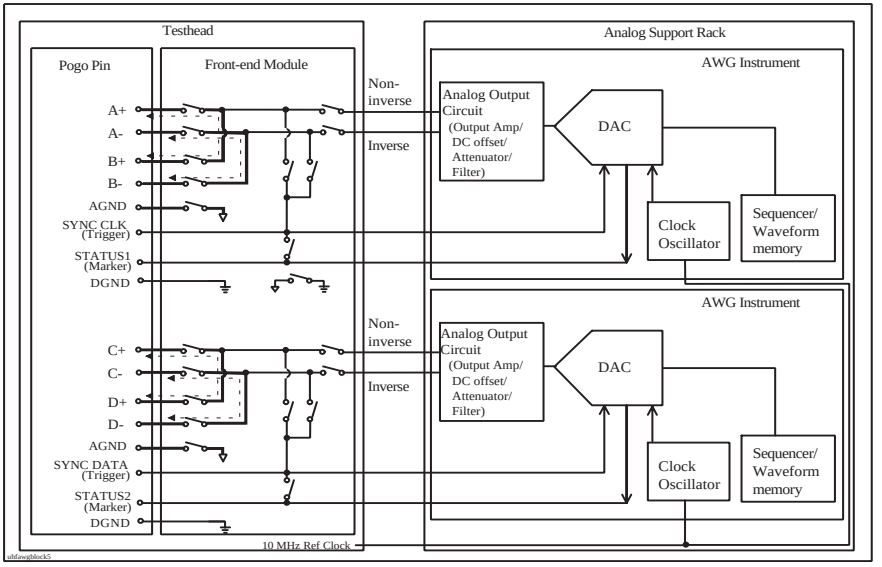


Figure 89 Loop Back Routes

The loop back route is designed so that the line impedance becomes 50 ohm exactly. As a result, the bandwidth of the loop back route extends up to 500 MHz (typical value). Hence, by using the loop back route, you can make a route that has better performance than using additional user relays on the DUT board.

AWG Instrument

The AWG instrument is installed in the analog support rack. The AWG instrument consists of the following blocks.

- Analog output circuit
- Digital-to-analog converter
- Clock ocsillator
- Sequencer and waveform memory

The following sections describe the functions of each block.

Analog Output Circuit

The analog output circuit has the following circuits.

- Attenuator for adjusting the amplitude of the output signal
- Low pass filter for removing harmonics from the output signal
- DC offset circuit
- Output amplifier

The ultra high speed AWG has two output modes. One is normal mode and the other is direct mode. The direct mode can generate a signal of higher frequency than the normal mode. In the direct mode, the DAC output propagates to the pogo pin not through the filter and DC offset circuit, but only the attenuator.

Digital-to-Analog Converter (DAC)

The analog-to-digital converter (DAC) converts the digital waveform data transferred from the waveform memory to the analog signal, according to the output sequence from the sequencer. The DAC converts the digital data to the analog signal according to the conversion clock provided by the clock oscillator.

Clock Oscillator

The clock oscillator generates the conversion clock and provides it with the DAC. The master clock of the SOC series is phased-locked with the clock oscillator.

Sequencer and Waveform Memory

The sequencer controls the output sequence of the waveform data stored in the waveform memory. The output sequence of the waveform data is specified in the sequence program that is contained in the sequence memory. The following information can be specified in the sequence program.

- Waveform memory area to output waveform signal.
- Sequence instruction. The following operations can be specified.
  - No operation (NOP instruction)

    After the waveform data specified in the current sequence program line is processed, the sequencer proceeds to the next line.
  - Halt after waveform (HALT instruction)

    After the waveform data in the current sequence program line is processed, the sequencer stops and waits for the next trigger.
  - Repeat waveform (RPT/RPTI instructions)

    The waveform data on the current sequence program line is repeated the specified number of times (RPT) or infinitely (RPTI).

Waveform Digitizers

There are two types of waveform digitizers available as follows:

- **High Resolution Digitizer** (2 MSample/s 16-bit)
  — Code name: **WDB**
- **High Speed Digitizer** (41 MSample/s 12-bit)
  — Code name: **WDA**

Waveform Digitizer Overview

The waveform digitizer can digitize the analog signal output from DUT, then store the digitized waveform data in the waveform memory in real-time. The digitizer sequencer controls the waveform memory area where data is stored, and the number of sample points.

The digitizers start waveform measurements by entering the external triggers. Generally, a digital channel is used for each digitizer as the external trigger source. A trigger signal must be supplied at the SYNC CLK pin. For more information of the synchronization trigger, see *"Synchronization Trigger"* on page 248.

When the digitizer starts, no initial discard points are stored. The digitizer stores the digitized waveform data with the specified number of sample points into the specified waveform memory area, according to the sequence program. The following figure shows the real-time waveform digitizing.

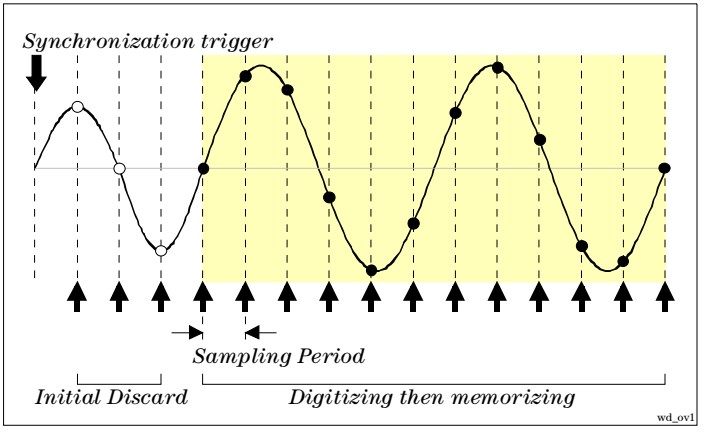


Figure 90 Real-Time Digitizing

The digitizer can also perform measurement at a higher frequency (equivalent sampling frequency) than the real-time digitizing, with the under-sampling technique called **Coherent Sampling**.

For effective measurement, this coherent sampling should use two master clocks. One master clock is for both the DUT (input signal to digitizer) and the synchronization trigger to the digitizer and one is for the sampling trigger of the digitizer.

To achieve coherent sampling, the measured signals should be periodic and you need to set the sampling period as follows:

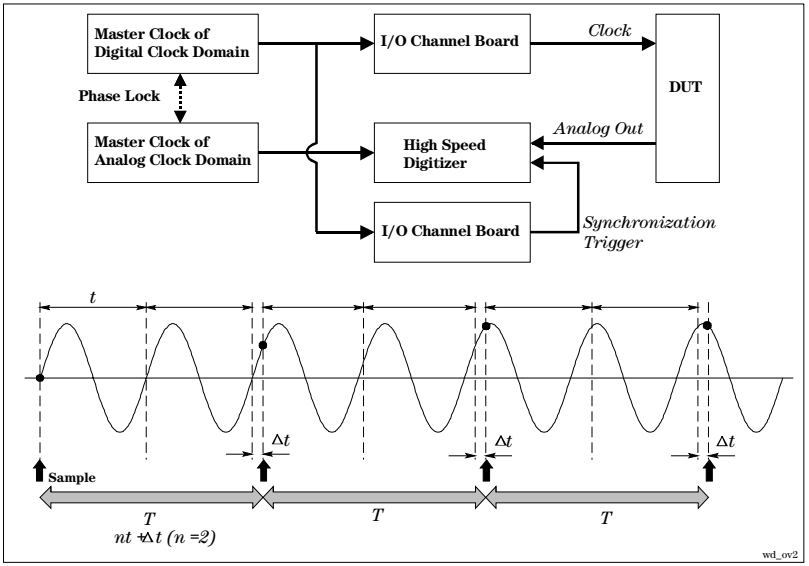


Figure 91 Coherent Sampling

Where, the sampling period (T) is slightly different (Δt) from a multiple of the signal period (t), that is T=nt+Δt. (Δt is called the equivalent sampling period.) The sampling is performed for each of the specified phase points on the measured signal.

You can observe or analyze the captured waveform data with the software interface, Mixed-Signal Tool.

NOTE The high resolution digitizer can upload previously measured data during the next measurement. It is designed to “capture” and “upload” different data at the same time. By using this feature, you can maximize throughput of data uploading.

The following tables show the key specifications of the waveform digitizers.

Specification	Value
Pin counts per module	8 single-ended or 4 differential
Resolution	16-bit (up to 24-bit with hardware averaging)
Sampling rate	8 ksps to 2.048 Msps
Waveform capture memory	1 M
Input mode	Single-ended or Differential
Input range	±6 V, ±3 V, ±1.5 V, ±0.75 V, ±0.2 V
DC offset range	±5 V
Common mode range	±6 V ±1/2 x range @1 Mohm single ended (with offset) ±6 V @50 ohm single ended (with offset) ±6 V @100 ohm differential (without offset)
Bandwidth @-3 dB	3 MHz @±6 V range, filter through (Characteristic)
Input impedance	1 Mohm, 50 ohm for single-ended 1 Mohm, 100 ohm for differential
Filter	Through, 6 kHz, 30 kHz, 150 kHz, 500 kHz
Min. capture data length	5
Sequencing - Number of steps - Functions	 256 - Halt when current measurement done - Continue next measurement
Number of Accu-mulations	256

Table 39 High Resolution Digitizer Key Specifications

Specification	Value
Pin counts per module	8 single-ended or 4 differential
Resolution	12-bit
Sampling rate	1 Msps to 41 Msps
Waveform capture memory	512 k
Input mode	Single-ended or Differential
Input range	±2 V, ±1 V, ±0.5 V, ±0.25 V
DC offset range	±4 V
Common mode range	±2 V @50 ohm, 37.5 ohm, 10 kohm single-ended and 100 ohm, 10 kohm differential (without offset) ±2 V @50 ohm, 37.5 ohm single-ended(with offset) ±6 V @10 kohm single-ended and differential (with offset)
Bandwidth @-3 dB	100 MHz @±0.5 V range, filter through (Characteristic)
Input impedance	10 kohm, 50 ohm, 37.5 ohm for single-ended 10 kohm, 100 ohm for differential
Filter	Through, 6.1 MHz(Video), 13 MHz, 26 MHz
Min. capture data length	3
Sequencing - Number of steps - Functions	 64 - Halt when current measurement done - Continue next measurement

Table 40 High Speed Digitizer Key Specifications

Theory of Operation

This section describes the theory of operation for digitizers. The following is the block diagram of the waveform digitizer.

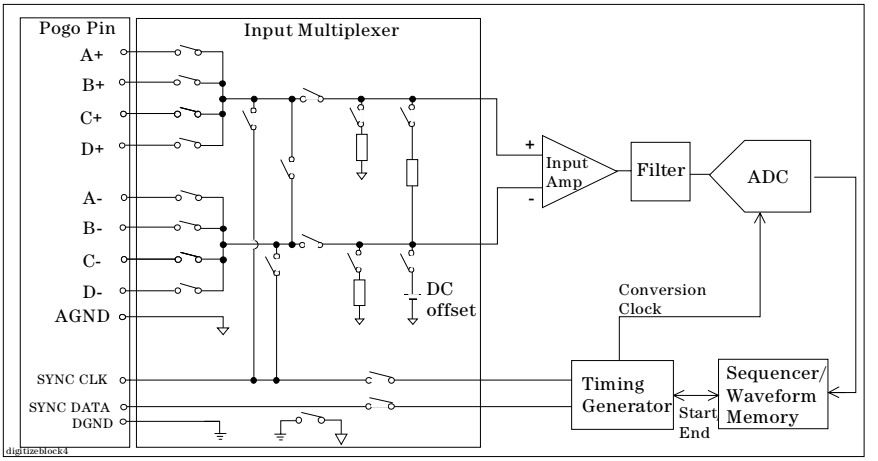


Figure 92 Digitizer Block Diagram

The waveform digitizer consists of the following blocks.

- Input Multiplexer
- Input Amplifier
- Low Pass Filter
- Analog-to-Digital Converter
- Timing Generator
- Sequencer and Waveform Memory

There is no SYNC DATA pin for the high speed digitizer.

The following sections describe the function of each block.

Input Multiplexer

The input multiplexer can make the following connections:

- Input routes
- DC routes
- Loop back routes

Input Routes

For measuring a single-ended signal, the signal is entered to one of the pogo pins. The input multiplexer connects the pogo pin and input amplifier by closing the internal relays between them.

For measuring a pair of differential signals, the signals are entered to one the following pairs of pogo pins: A+ and A-, B+ and B-, C+ and C-, or D+ and D-. The input multiplexer connects a pair of pogo pins and input amplifier by closing the internal relays between them.

When a pogo pin or a pair of pogo pins is connected with an input amplifier, the input multiplexer connects resistances with the route to determine the input impedance. The following figure shows available input impedance for the high speed digitizer and high resolution digitizer.

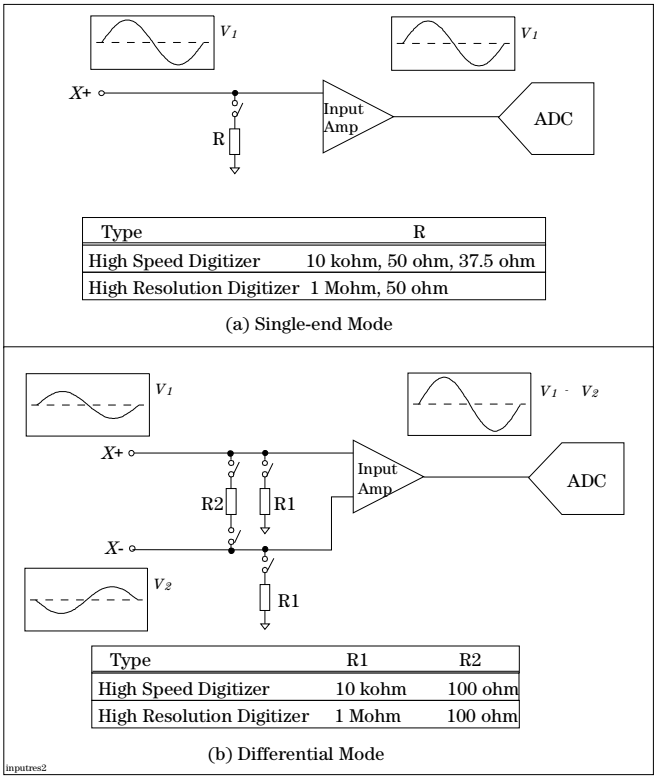


Figure 93 Input Resistance

DC Routes

The input multiplexer can make the route between a pogo pin and the SYNC CLK pin. This enables DC measurement by using a Pin PMU on a digital channel connected with the SYNC CLK pin. Hence, if you wire a digital channel with the SYNC CLK pin on the DUT board, you can perform DC measurement at the DUT pin connected to a digitizer by using a Pin PMU. The following figure shows the possible routes between the pogo pins and SYNC CLK pin, which are represented with bold lines. When the DC route is made, the input amplifier is disconnected from any pogo pins.

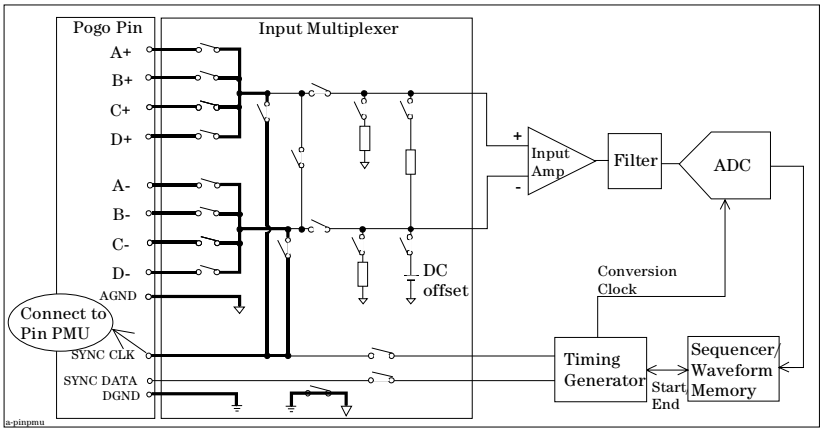


Figure 94 DC Routes

Loop Back Routes

The input multiplexer can make the loop back route between any pogo pins (except for SYNC CLK and SYNC DATA pins). When the loop back route is made, the input amplifier is disconnected from the input multiplexer. In the following figure, the possible loop back routes are represented with bold lines.

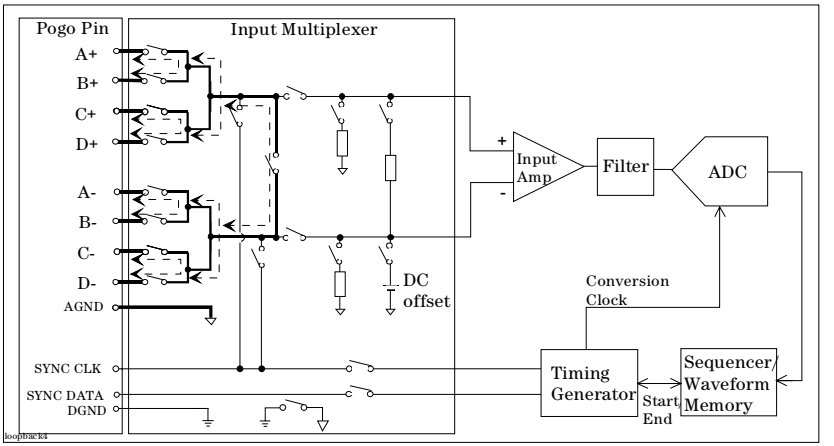


Figure 95 Loop Back Routes

The loop back route is designed so that the line impedance becomes 50 ohm exactly. As a result, the bandwidth of the loop back route extends up to 150 MHz (typical value) for the high resolution digitizer, and 195 MHz (typical value) for the high speed digitizer. Hence, by using the loop back route, you can make a route that has better performance than using additional user relays on the DUT board. Note that the bandwidth of the loop back route between A+/B+/C+/D+ and A-/B-/C-/D- pins is narrower than the above typical values.

For example, to test a DUT, you may need to change tester resources connected with a DUT pin, depending on test items. The following figure shows an example. The DUT needs a high speed digitizer for a test item and a high reso-

lution digitizer for another test item for the Aout pin. When K1 and K3 are closed and K2 is open, the signal from the Aout pin can be measured by the high speed digitizer. When K1, K2, K4, and K5 are closed and K3 is open, the signal from the Aout pin can be measured by the high resolution digitizer. Use of the loop back route can make the measurement performance better than when user relays are used on the DUT board for changing the high speed digitizer and high resolution digitizer.

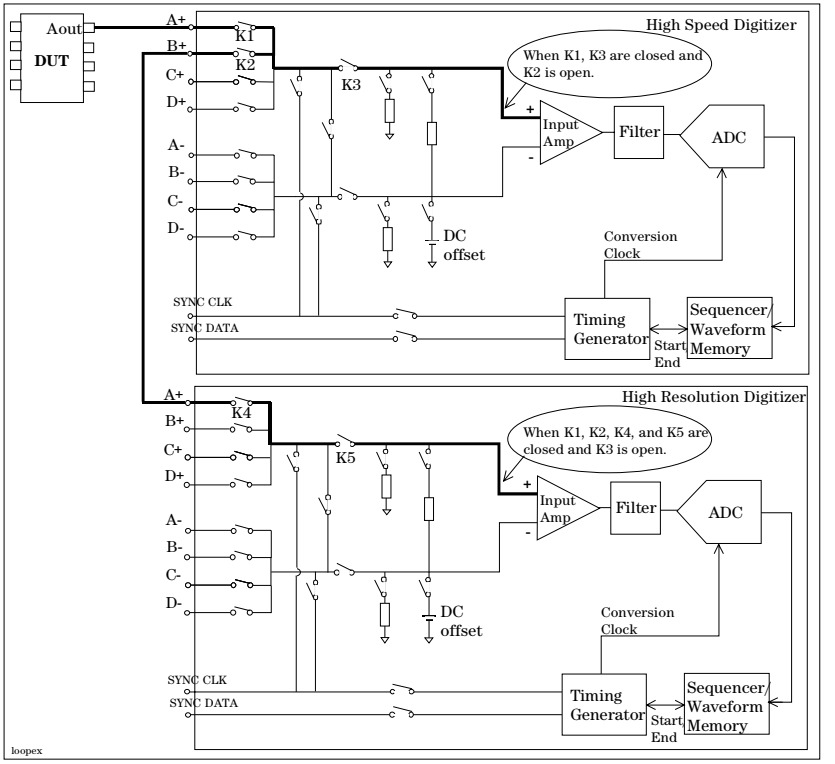


Figure 96 Example for Using Loop Back Route

Input Amplifier

The input amplifier determines the input voltage range. Any input voltage ranges are normalized to a certain voltage range at the output of the input amplifier.

If the signal to be measured includes a DC component and you want to measure only AC components, you can eliminate the DC component by setting the DC offset voltage. The input amplifier eliminates the DC component according to your setting for the DC offset voltage. This maximizes the measurement dynamic range for AC components.

Filter

The digitizer has some kinds of low pass filters for anti-aliasing according to the band of measured signals. The filter removes harmonics from the input signal.

Analog-to-Digital Converter

The analog-to-digital converter samples the analog signal according to the conversion clock provided by the timing generator and converts the level of the analog signal to digital data. The digital data is stored in the waveform memory.

Timing Generator

The master clock and trigger signal are input to the timing generator. After receiving the trigger signal, the timing generator starts to generate the conversion clock by dividing the master clock and feeds the conversion clock to the ADC. The timing generator also sends the start signal to the sequencer. The timing generator stops generating the conversion clock when the sequencer is halted.

The timing generator contains a delay counter and delay vernier. By using them, the timing generator controls the delay time from when the trigger signal arrives to when waveform measurement starts.

Sequencer and Waveform Memory

The sequencer controls storage of digitized data into the waveform memory. The conditions for storing digitized data are specified in the sequence program that is contained in the sequence memory. The following conditions can be specified in the sequence program.

- Number of initial discard points
- Waveform memory area where digitized data is stored
- Averaging times (High resolution digitizer only)
- Sequence instruction that specifies whether to halt measurement after the sequence on the current line is completed (HALT instruction) or to continue to the next line (NOP instruction)

Sampler

There is one type of sampler available as follows:

- **Dual High Speed Sampler** (1 GHz 12-bit)
  — Code name: **SPA**

Sampler Overview

The sampler is a special module in the waveform digitizers. The sampler can capture very high frequency analog signals that cannot be measured by general waveform digitizers described in the previous section.

The sampler can record periodic signals only. The periodic signal is sampled and held by the high bandwidth sampling head, then digitized by an internal analog-to-digital converter that works the same way as the digitizer. The digitized data can be stored in the waveform memory. The digitized data can be averaged for the same phase point. The sampler sequencer controls the waveform memory area where digitized data is stored, and the number of sample points.

A sampler module has two channel units. The two channels can operate by sharing the timing generator, sequencer, and waveform memory simultaneously. Hence, the two channels can measure two analog signals with a very tight timing skew (typical ±100 ps). To perform highly accurate two-channel measurements, you should connect the input pins of the sampler to DUT output pins with coaxial cables or patterns that have the same electrical length on the DUT board, and use the same voltage range for both channels.

The samplers start waveform measurements by entering the external triggers. Generally, a digital channel is used for each sampler (two channels) as the external trigger source. A trigger signal must be supplied at the SYNC CLK pin. For more information of the synchronization trigger, see *"Synchronization Trigger"* on page 248.

In the sampler, the sampling period (T) is slightly different (Δt) from a multiple of the signal period (t), that is, T=nt+Δt. (Δt is called the equivalent sampling period.)

This under-sampling technique is called **Coherent Sampling**. The sampling is performed for each of the specified phase points on the measured signal, then repeated and averaged for each phase point.

To obtain a very short equivalent sampling period (Δt), the sampling period (T) must be freely set. In this case, the coherent sampling should use two master clocks. Two master clocks are used, one for both the DUT (input signal to sampler) and the synchronization trigger to the sampler and one for the sampling clock of the sampler.

The shortest equivalent sampling period for using two master clocks is 1 ps.

The following figure illustrates coherent sampling with two master clocks:

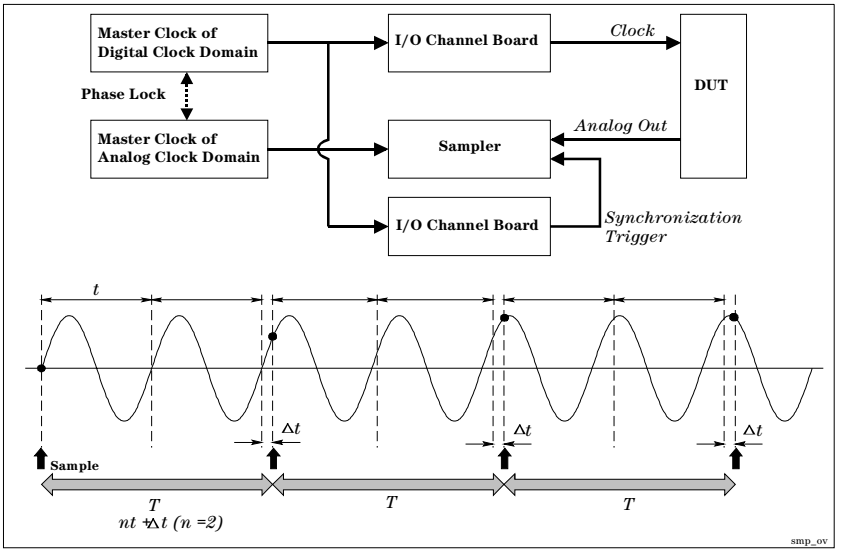


Figure 97 Coherent Sampling

You can observe or analyze the captured waveform data with the software interface, Mixed-Signal Tool.

NOTE The dual high speed sampler can upload previously measured data during the next measurement. It is designed to "capture" and "upload" different data at the same time. By using this feature, you can maximize throughput of data uploading.

The following table shows the key specifications of the sampler.

Specification	Value
Pin counts per module	4 single-ended (2 parallel test)
Resolution	12 bit
Sampling rate	8 ksps to 1 Msps
Waveform capture memory	1M (512 K per channel)
Input mode	Single-ended
Input range	±1 V, ±0.2 V, ±0.02 V
DC offset range	±1 V, ±0.2 V, ±0.02 V
Common mode range	±1 V, ±0.2 V, ±0.02 V
Max. input frequency	1 GHz
Input impedance	50 ohm
Min. capture data length	16
Sequencing - Number of steps - Functions	 256 - Halt when current measurement done - Continue next measurement
Number of Accumulations	256

Table 41 Sampler Key Specifications

Theory of Operation

This section describes the theory of operation for a sampler. The following is the block diagram of the sampler.

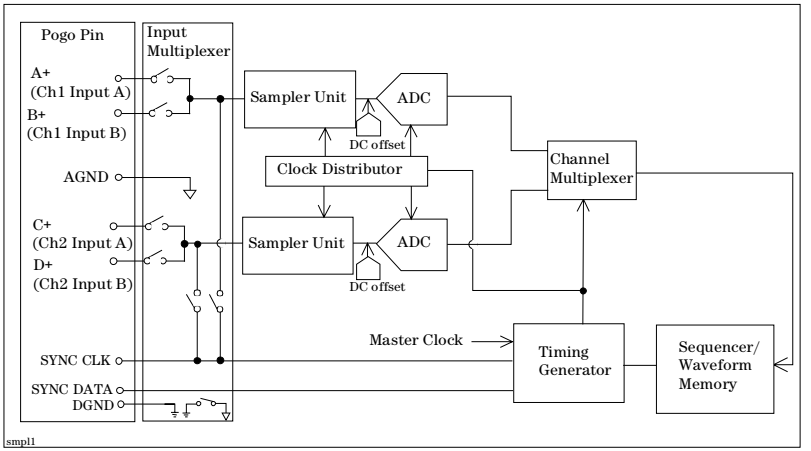


Figure 98 Sampler Block Diagram

The sampler consists of the following blocks.

- Input multiplexer
- Sampler unit
- Analog-to-digital converter (ADC)
- Clock distributor
- Channel multiplexer
- Timing generator
- Sequencer and waveform memory

One sampler board has two channels. Each channel has its own sampler unit and analog-to-digital converter (ADC). Each channel has two input pins. The clock distributor, channel multiplexer, timing generator, sequencer, and

waveform memory are shared between two channels. The SYNC CLK and SYNC DATA pins are also shared between two channels.

You can use one channel only or two channels simultaneously.

The following sections describe function of each block.

Input Multiplexer

The input multiplexer makes the following connections.

- Input routes
- DC routes
- Loop back routes

Input Routes

To measure a signal entered to the pogo pin, the input multiplexer makes the route between the specified pogo pin and the sampler unit.

Only the single-ended signal can be entered to the pogo pin.

DC Routes

The input multiplexer can make the route between a pogo pin and the SYNC CLK pin. This enables DC measurement by using a Pin PMU on a digital channel connected with the SYNC CLK pin. Hence, if you wire a digital channel with the SYNC CLK pin on the DUT board, you can perform DC measurement at the DUT pin connected to a sampler by using a Pin PMU. The following figure shows the possible routes between the pogo pins and SYNC CLK pin, which are represented with bold lines. When the DC route is made, the sampler unit is disconnected from any pogo pins.

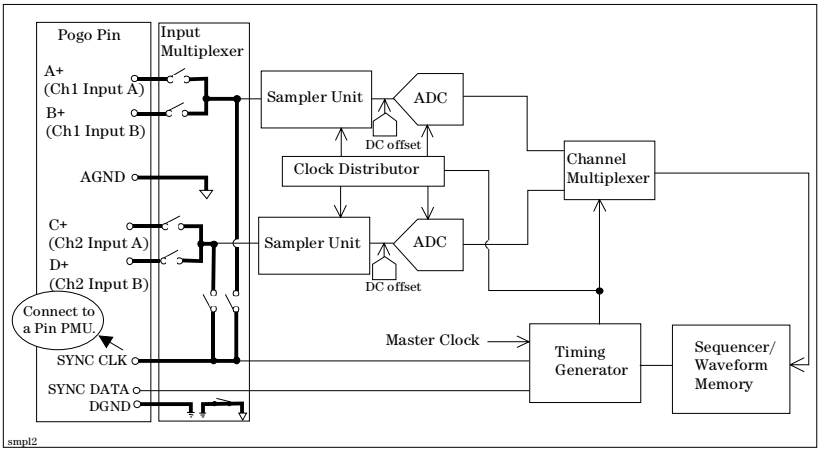


Figure 99 DC Routes

Loop Back Routes

The input multiplexer can make the loop back route between adjacent pogo pins (A+ and B+, or C+ and D+). When a loop back route is made, the loop back route is disconnected from other routes. Hence, you can make multiple loop back routes, or also make a loop back route and another route (output route or DC route) using other pins at the same time. In the following figure, the possible loop back routes are represented with bold lines.

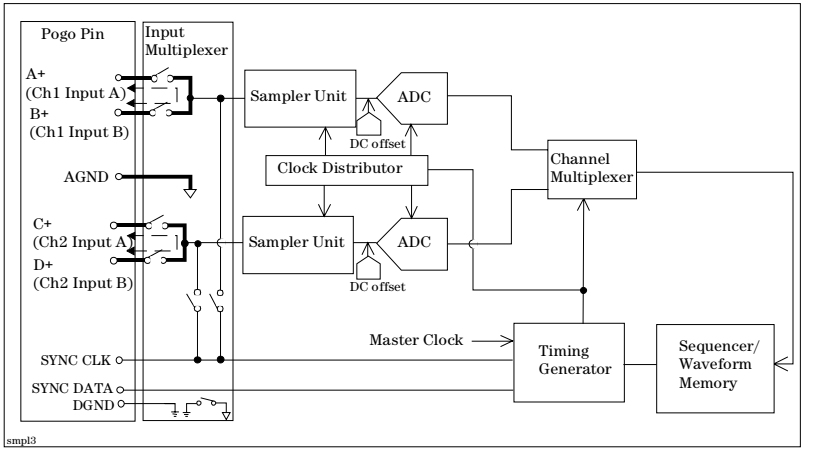


Figure 100 Loop Back Routes

The loop back route is designed so that the line impedance becomes 50 ohm exactly. As a result, the bandwidth of the loop back route extends up to 500 MHz (typical value). Hence, by using the loop back route, you can make a route that has better performance than using user relays for changing the connections in the test circuit.

Sampler Unit

The sampler unit periodically samples the high speed input signal and holds it until the analog-to-digital converter converts it into digital data. The sampling period is set to a multiple of the input signal plus a small amount of time. Thus, the frequency of the input signal is converted to one that is low enough to enable the analog-to-digital converter to convert the level of the input signal into digital data.

Analog-to-Digital Converter (ADC)

The analog-to-digital converter (ADC) converts the level sampled by the sampler unit to the digital data according to the conversion clock provided by the clock distributor.

Clock Distributor

The clock distributor receives the conversion clock from the timing generator, adjusts the edge timing and provides the clock to the sampler unit and the ADC in both channels.

Channel Multiplexer

The channel multiplexer separately transfers digital data from ADCs in both channels to the waveform memory.

Timing Generator

The master clock and trigger signal are input to the timing generator. After receiving the trigger signal, the timing generator starts to generate the conversion clock by dividing the master clock and feeds the conversion clock to the ADC and sampler unit via the clock distributor. The timing generator also sends the start signal to the sequencer. The timing generator stops to generate the conversion clock when the sequencer is halted.

The timing generator contains the delay counter and delay vernier. By using them, the timing generator controls the delay time from when the trigger signal arrives to when waveform measurement starts.

When you use two channels simultaneously, the sampling period, start timing, and stop timing of measurement are the same for the two channels because the timing generator and trigger input pins are shared.

Sequencer and Waveform Memory

The sequencer controls the storage of sampled and digitized data into the waveform memory. The conditions for storing digitized data are specified in the sequence program that is contained in the sequence memory. The following conditions can be specified in the sequence program:

- Number of initial discard points
- Waveform memory area where digitized data is stored
- Averaging times
- Sequence instruction that specifies if the measurement is halted after the sequence on the current line is completed (HALT instruction) or continued to the next line (NOP instruction)

When you use two channels simultaneously, the sequence program is shared between two channels.

Time Interval Analyzer

There is one type of TIA available as follows:

- **High performance TIA** — Code name: **TIA**
- **General purpose TIA** — Code name: **TIA**

These TIAs provide the same functions. Some specifications are different between these TIAs. For specifications, see Table 42 and Table 43.

TIA Overview

The Time Interval Analyzer (TIA) performs time measurements for digital or analog signals, and stores the results.

Signals can be input to one TIA module through two input lines as follows:

- Channel 1 (Start channel at propagation delay measurement)
- Channel 2 (Stop channel at propagation delay measurement)

The input signals to these input channels are converted to digital signals with the specified threshold levels at the front end of the input channels.

The TIA can perform the following four kinds of interval measurements available:

- Pulse width on either channel 1 (PW)
- Pulse period on either channel 1 (PER)
- Frequency of a signal on either channel 1 (FREQ)
- Propagation delay between edges on dual channels (PD)

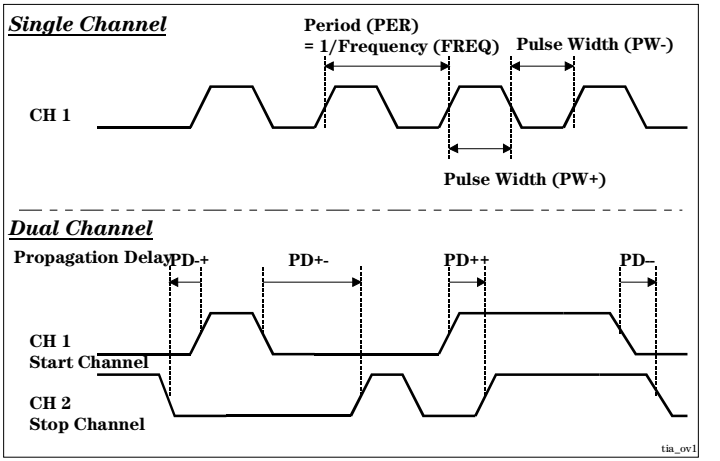


Figure 101 TIA Measurement Functions

The TIA can measure intervals with the specified numbers of samples and store them into the local memory, then return the following data calculated from the raw sampled data as the measurement results:

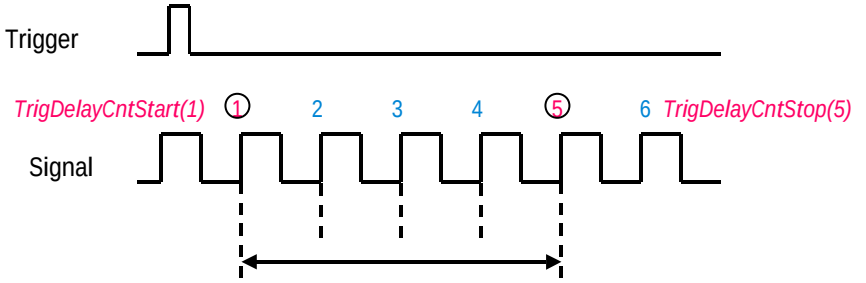
- Maximum value
- Minimum value
- Jitter RMS (standard deviation)
- Mean (averaged value)

Edges to Start and Stop Measurement

For edge types determined by the `measureMode` setting, the TIA starts counting edges for start and/or stop channels to perform the time measurement after the trigger signal is detected. `trigDelayCntStart` and `trigDelayCntStop` are used to specify at which edges to start and stop the measurement. They have different meanings depending on which measurement is performed:

- Period/Frequency Measurement

This mode is used to measure the period or frequency of a periodic signal.



The TIA measures this interval, then divides the measured interval by 4 (5-1) to get averaged period/frequency.

Figure 102 `TrigDelayCnt` Parameters for Period/Frequency Measurement

For PER or FREQ, after the trigger is detected, the TIA counts the rising edges of the signal to start and stop the measurement using `TrigDelayCntStart` and `TrigDelayCntStop`. In this case, the TIA first measures the interval from the edge determined by `TrigDelayCntStart` to the edge determined by `TrigDelayCntStop`, then divides the interval by the number of cycles to get an averaged period/frequency. In the above example, the interval to be measured includes 4 (5-1) cycles of the clock. Therefore, to get an averaged period, the measured interval is divided by 4.

NOTE By default, 1 is set to both `TrigDelayCntStart` and `TrigDelayCntStop`. To specify one cycle of a waveform to be measured, `TrigDelayCntStop` must be greater than `TrigDelayCntStart`.

- Pulse Width Measurement

This mode is used to measure the negative or positive pulse width of a signal.

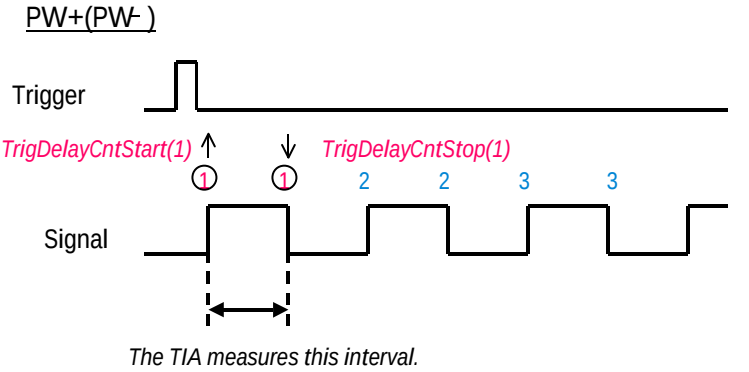


Figure 103 `TrigDelayCnt` Parameters for Pulse Width Measurement

For PW+ or PW-, after the trigger is detected, the TIA counts rising edges and falling edges, respectively. The TIA measures the interval from the edge for `TrigDelay-CntStart` to the edge for `TrigDelayCntStop`.

– For PW+, `TrigDelayCntStart` determines at which rising edge to start the measurement and `TrigDelayCntStop` determines at which falling edge to stop the measurement.

  For PW-, `TrigDelayCntStart` determines at which falling edge to start the measurement and `TrigDelayCntStop` determines at which rising edge to stop the measurement.

In the above example, as `TrigDelayCntStart(1)` and `TrigDelayCntStop(1)` are specified, the TIA measures from the first rising edge of the signal after the trigger to the first falling edge of the signal after the rising edge.

NOTE You can set number of sampling points by using `POINTS`. In this case, an interval of sampling points is more than 30 µs.

- Propagation Delay Measurement

This mode is used to measure the time difference between edges of two input channels:

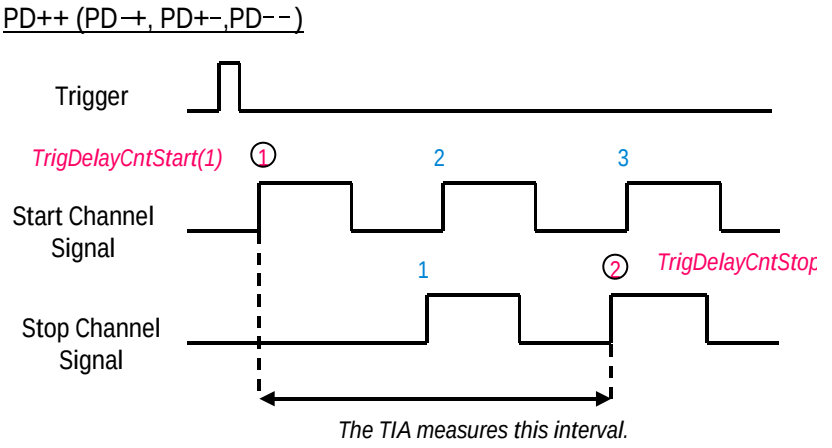


Figure 104 `TrigDelayCnt` Parameters for Propagation Delay Measurement

For propagation delay measurement, the TIA counts edges determined by the measurement mode for start channel and stop channel, respectively.

In the above example, as `TrigDelayCntStart(1)` and `TrigDelayCntStop(2)` are specified, the TIA measures the propagation delay from the first rising edge of the start channel signal to the second rising edge of the stop channel signal after the trigger.

Trigger Mode and Number of Measurements

The TIA starts the interval measurements when the specified edge (rising or falling edge) of the trigger is detected. The TIA has two trigger modes the auto trigger mode and the external trigger mode.

- **Auto Trigger mode**

  This mode uses the edge of the input signal to channel 1 or 2 as the trigger, as follows:

  – **ARM on Start**:

  The TIA starts the interval measurements from the next pulse after the specified edge of the channel 1 input signal is detected as a trigger.
  For the dual channel measurement, the TIA measures the interval from the specified edge on channel 1 to the specified edge on channel 2. However, if the TIA detects the edge on channel 2 before the edge on channel 1, the measurement data is a negative value.

  This function is available for PW/PER/FREQ measurements on channel 1 and PD measurements.

  – **ARM on Stop**:

  The TIA starts the interval measurements from the next pulse after the specified edge of the channel 2 input signal is detected as a trigger.
  For the dual channel measurement, the TIA measures the interval from the specified edge on channel 1 to the specified edge on channel 2. However, if the TIA detects the edge on channel 2 before the edge detection on channel 1, the measurement data is a negative value.

  This function is available for PD measurements.

  – **ARM Start First**:

  The TIA starts the interval measurements from the next pulse after the specified edge of the channel 1 input signal is detected as a trigger. This mode requires a minimum 1 ns setup time.
  For the dual channel measurement, the TIA measures the interval from the specified edge on channel 1 to the specified edge on channel 2. Even if there are some edges on channel 2 before the edge

detection on channel 1, the edges on channel 2 are ignored. Thus, the measurement data is always a positive value.

This is available for PD measurements.

- **External Trigger mode**

  This mode uses the edge of the external trigger as the arming trigger. The TIA starts the interval measurements from the next pulse after the specified edge of the external trigger is detected as an arm.

  This mode is available for any measurement.

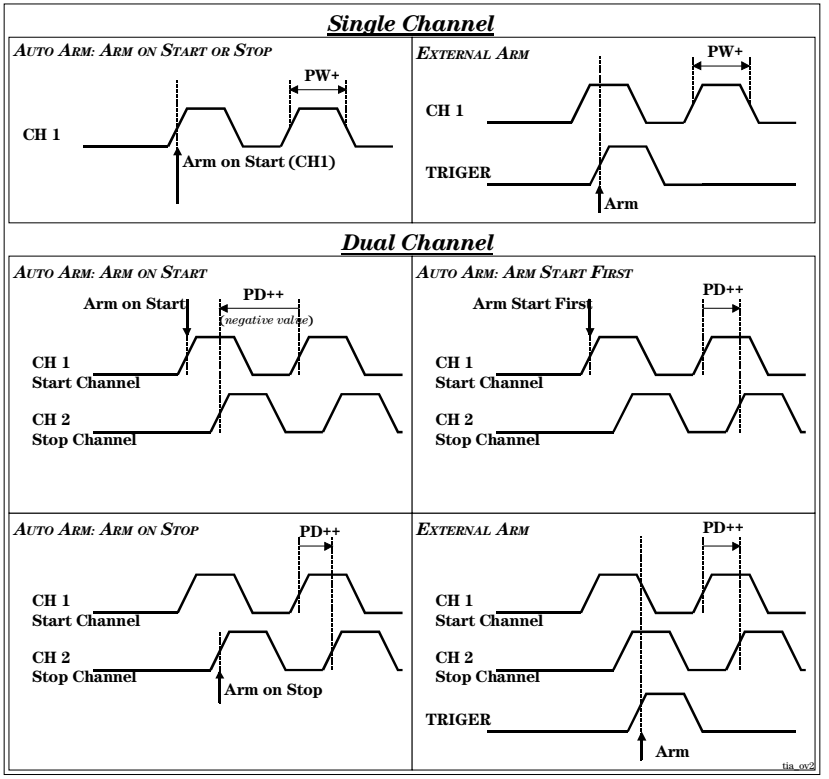
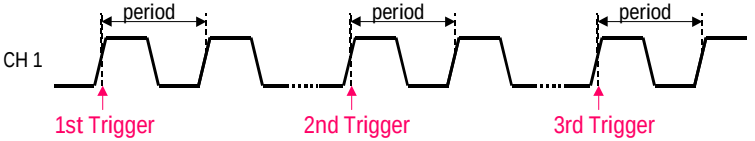


Figure 105 Examples of Trigger Modes

For a periodic signal, the jitter test has to measure multiple periods that are not averaged. To perform a single period measurement multiple times for EXT(External) trigger mode, the number of measurement times must be set to `points` and the trigger for each measurement must be specified. In this case, after a measurement is done, the trigger for the next measurement must be set at 30 µs or later.

If the trigger mode is AUTO, the measurement is started at a specified edge of the signal to be measured. In this case, if 2 or more is set `points`, that is, multiple measurements are performed, the TIA automatically starts the second and later measurements.

● **trigMode: AUTO, trigEdge: RISING**



● **trigMode: EXT, trigEdge: RISING**

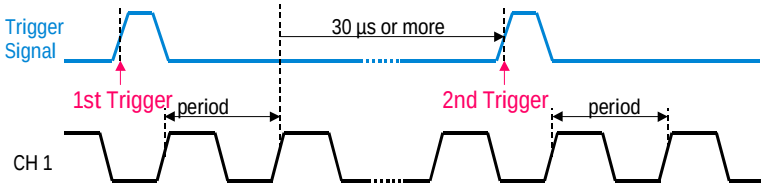


Figure 106 `trigMode` and `trigEdge`

The following example shows the relationship of `TrigDelayCntStart`, `TrigDelayCntStop`, and `points` for EXT trigger mode:

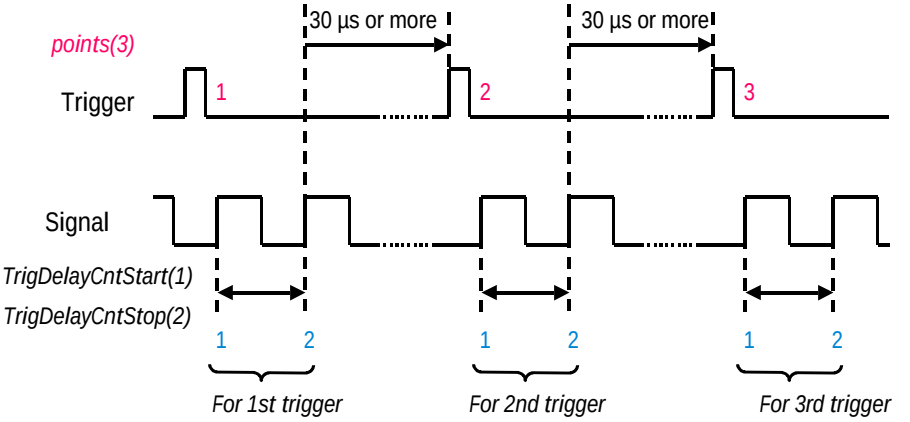


Figure 107 Measuring Multiple Intervals

In the above example, `TrigDelayCntStart(1)` and `TrigDelayCntStop(2)` specify one cycle of the waveform to measure the non-averaged period after each trigger. That is, the number of triggers must be more than or equal to `points`.

TIA Key Specifications

The following tables show the key specifications of the High Performance TIA.

Specification	Value
Pin counts per front-end module	7 input pins (with signal loopback) 2 trigger pins
Number of triggers input	1 input to each TIA instrument
Number of channels per TIA instrument	2 channels

Table 42 High Performance TIA Key Specifications

Specification	Value
Max. input frequency	960 MHz (Signal input 50 ohm) (Characteristics)
Input voltage range Signal input Trigger (arming) input	 -3 V to +7 V -1.5 V to +2.5 V
Threshold voltage (Vth) range Number of threshold per pin Resolution	-2 V to +6 V (|Vin - Vth| ≤ 7 V) 1 1 mV
Input impedance Signal input Trigger (arming) input	 50 ohm to termination voltage 10 kohm to ground 50 ohm to ground
Termination voltage (Vterm) range Resolution	-2 V to +6 V (|Vin - Vterm| ≤ 2 V) 1 mV
Min. pulse width Signal input (50 ohm)	 750 ps@2 Vpp, single-shot (Characteristics)
Slope	Positive, Negative
Measurement mode	Period, Frequency, Pulse Width, Propagation Delay
Range	-2.5 s to +2.5 s
Resolution	0.8 ps @single-shot
Trigger functions	Arm on Stop, Arm on Start, Arm Start First

Table 42 High Performance TIA Key Specifications

The following tables show the key specifications of the General Purpose TIA.

Specification	Value
Pin counts per front-end module	7 input pins (with signal loopback) 2 trigger pins
Number of triggers input	1 input to each TIA instrument
Number of channels per TIA instrument	2 channels
Max. input frequency Signal input 50ohm Signal input 10kohm	 400MHz(Characteristics) @2Vpp sin wave 200MHz(Characteristics) @2Vpp sin wave
Input voltage range Signal input Trigger (arming) input	 -3 V to +7 V -1.5 V to +2.5 V
Threshold voltage (Vth) range Number of threshold per pin Resolution	-2 V to +6 V ($\|Vin - Vth\| \leq 7$ V) 1 1 mV
Input impedance Signal input Trigger (arming) input	 50 ohm to termination voltage 10 kohm to ground 50 ohm to ground
Termination voltage (Vterm) range Resolution	-2 V to +6 V ($\|Vin - Vterm\| \leq 2$ V) 1 mV
Min. pulse width Signal input (50 ohm)	 1.25 ns@2 Vpp, single-shot (Characteristics)
Slope	Positive, Negative
Measurement mode	Period, Frequency, Pulse Width, Propagation Delay
Range	-2.5 s to +2.5 s

Table 43 General Purpose TIA Key Specifications

Specification	Value
Resolution	0.8 ps @single-shot
Trigger functions	Arm on Stop, Arm on Start, Arm Start First

Table 43 General Purpose TIA Key Specifications

Theory of Operation

This section describes the theory of operation for the TIA. The following is simplified block diagram of the TIA.

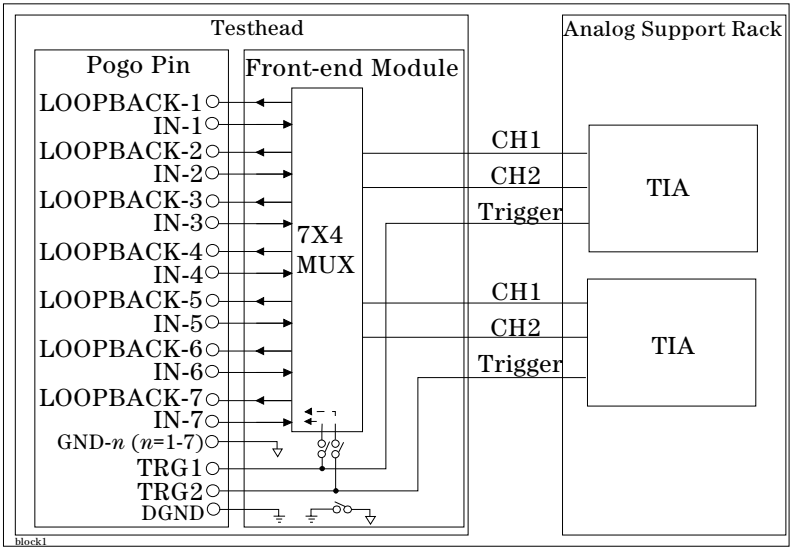


Figure 108 Front-end Module and TIA Instrument

The TIA is separated into two blocks, for the front-end module and the TIA instrument. The front-end module is in the testhead. The TIA instrument is in the analog support rack. One front-end module supports up to two TIA instruments.

The front-end module has seven signal input pins and two trigger input pins. The 7x4 multiplexer inside the front-end module routes one or two input pins among seven input pins to the input channels (CH1 and CH2) of each TIA instrument. The TIA instrument performs the time interval measurement for the signals entered to CH1 and CH2 of the TIA. The trigger input pin is routed to each TIA instrument to send the arming trigger signal. For single channel measurement (PW,PER,FREQ), input pins are connected only to the CH1. For dual channel measurement (PD), input pins are connected to the CH1 and CH2.

The following sections describe the front-end module and TIA instrument in detail.

Front-end Module

The following is the block diagram of the front-end module.

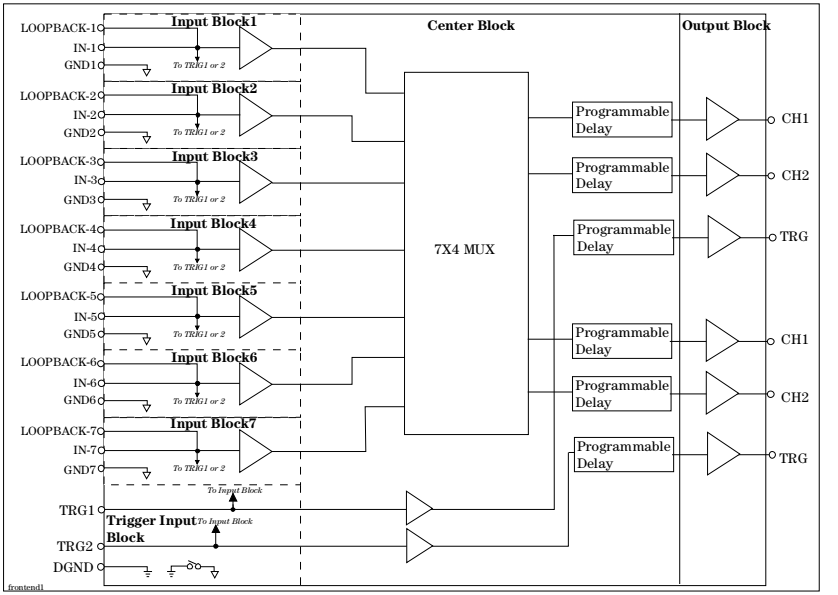


Figure 109 Front-end Module Block Diagram

The front-end module consists of the following three kinds of blocks:

- Input block
- Center block
- Output block

The following sections describe the functions of each block.

Input Block

In the front-end module, there are seven input blocks. One input block corresponds to one input pin. There is one trigger input block for two trigger pins. The grounds of the input blocks are separated from each other. This is to prevent interference among the signals entered to the input pins.

Below is the block diagram of the input block for one input pin.

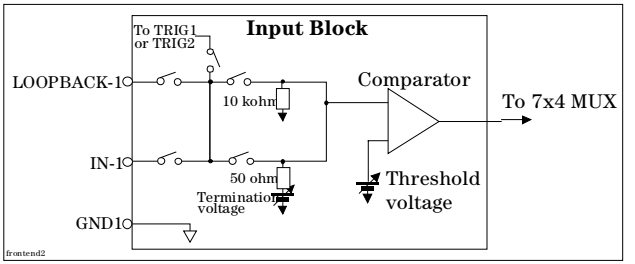


Figure 110 Input Block

The input block has the following functions:

- Receives the signal at the input pin and converts the signal to the two level digital signal (high and low) according to the specified threshold voltage at the comparator.

- Determines the input impedance.

  You can select 10 kohm or 50 ohm as the input impedance. For 50 ohm, you can specify the termination voltage.

- Makes the DC routes.

  The specified input pin is connected to the specified trigger pin. Hence, you can perform DC measurement at the input pin by using the Pin PMU if you wire the digital channel to the trigger pin on the DUT board.

  When the DC route is made, the DC route is disconnected from other routes.

- Makes the loop back routes.

  Each input block has an input pin and a loop back pin. The input pin can be routed to the loop back pin. When a loop back route is made, the loop back route is disconnected from other routes. Hence, you can make multiple loop back routes, or also make a loop back route and another route (input route or DC route) using other pins at the same time.

  The loop back route is designed so that its line impedance becomes exactly 50 ohm. As a result, the band width of the loop back route extends up to 700 MHz (typical value). Hence, by using the loop back route, you can make a route that has better performance than using additional user relays on the DUT board.

Center Block

The center block has the following functions:

- Routes one or two input pins among seven input pins to the TIA instrument. For single channel measruement (PW, PER, FREQ), only CH1 is routed to a pin. CH2 is only routed to a pin for dual channel measruement (PD).

  If two TIA instruments are connected with the front-end module, the center block can route one or two input pins to one TIA instrument and another one or two input pins to the other TIA instrument.
- Compensate the skew between the input pins and between the input pin and the trigger pin.

  Because the length of the routes inside the front-end module are different depending on the input pins and trigger pins, the skew happens between the input pins and between the input pin and the trigger pin. The programmable delay in the center block compensates the skew.
- Comparator for the trigger (arming signal) input

  The input impedance of the trigger is 50 ohm. The threshold level of the comparator of the trigger pin is fixed to 0.0 V. The level of the trigger (arming) signal must be within -1.5 V to +2.5 V (@50 ohm termination).

Output Block

The output block outputs the signals and trigger signals with 50 ohm impedance to the TIA instruments.

TIA Instrument

The following is the simplified block diagram of the TIA instrument.

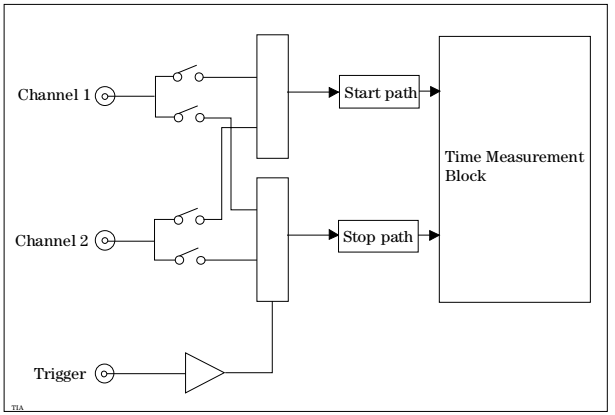


Figure 111 TIA Instrument Block Diagram

The TIA instrument has two signal inputs and one trigger input. Each signal input can be routed to the internal paths for the start and stop signals. This enables events such as pulse width or pulse period to be measured on a single input with one channel only.

Two signal inputs must be used for measuring propagation delay.

The trigger signal determines the measurement start timing as an arming trigger.

Synchronization

This section provides the following information for synchronizing between the digital channel operation and the analog module operation (except for TIA):

- Synchronization concepts
- Technical data of the synchronization trigger
- How to adjust the synchronization timing
- How to remove the synchronization uncertainty that occurs in the high speed analog modules
- Special synchronization function for high speed AWGs and dual high speed samplers

Synchronization Concepts

An analog module starts the operation when it receives a trigger signal. The trigger signal for the analog module is provided by a digital channel generally. All analog modules have dedicated trigger input pins. For sending the trigger signal, you have to connect the digital pin that provides the trigger signal and the trigger input pin of the analog module on the DUT board.

Trigger-to-Delay and Uncertainty

Analog modules start measurement or waveform generation after a certain delay from the time the trigger signal is received. This delay time is called **trigger-to-signal delay**. Each analog module has a dedicated value of delay time. The analog module's timing calibration supported by the system compensates the trigger-to-signal delay in each analog module. After the calibration, the trigger-to-signal delay will become the fixed value for each analog module.

The following table shows the fixed value of the trigger-to-signal delay, the accuracy of the trigger-to-signal delay, and uncertainty of the analog module's start timing.

Analog Module	Trigger-to-Signal Delay	Accuracy	Uncertainty
High Resolution AWG	1000 ns	±250 ns	±1 master clock period
High Speed AWG	200 ns	±1 ns	0 to ±1 master clock period
Ultra High Speed AWG	110 ns	±(450 ps + OTA)	± 1 sampling clock
High Resolution Digitizer	0 ns	±500 ns	±1 master clock period
High Speed Digitizer	50 ns	±1 master clock period	0 to ±1 master clock period
Dual High Speed Sampler	70 ns	±1 ns	0 to ±1 master clock period

Table 44 Trigger-to-Signal Delay, Accuracy, and Uncertainty

Where, "**1 master clock period**" means one period of the master clock used for the analog module.

"**Accuracy**" in the above table means a fixed delay that could not be compensated by the analog module's timing calibration. Further, it has repeatability; if a test is done under certain conditions of the analog module, the analog module always starts "Trigger-to-Signal Delay ± the fixed delay" after receiving the trigger signal when the "**Uncertainty**" is zero.

"**Uncertainty**" means the dispersion of the start timing of the analog module. It has no repeatability; the start timing of the analog module may be different even if the test is done under the same conditions. The analog module starts in the uncertainty range around the "Trigger-to-Signal Delay ± the fixed delay" point after receiving the trigger signal. See the following figure.

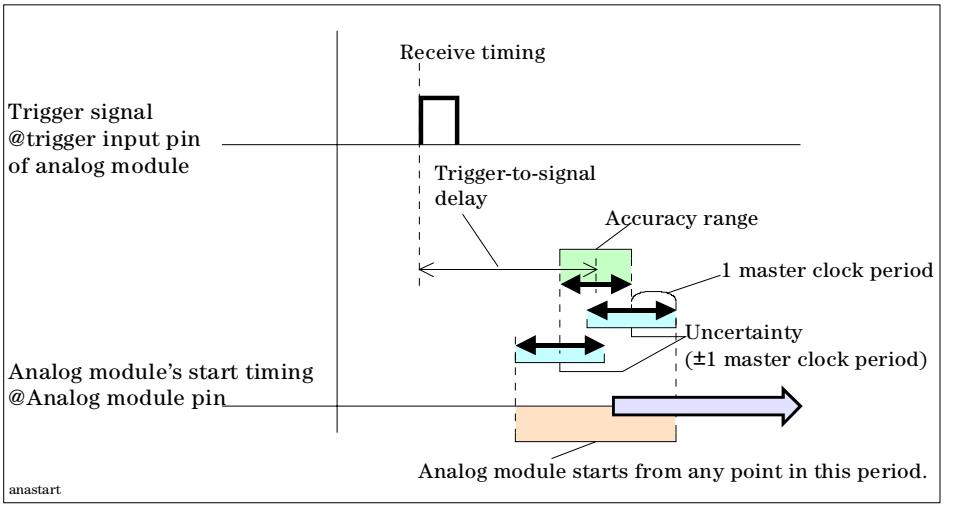


Figure 112 Start Timing of Analog Module after Receiving Trigger

If a test requires highly accurate synchronization between the digital channel operation and an analog module operation, you need to decide the edge position of the trigger signal that will be sent to the analog module, taking account of the "Trigger-to-Signal Delay", "Accuracy", and "Uncertainty" for the start timing of the analog module. Therefore, you should consider whether the dispersion for the start timing of the analog module such as shown in the above figure has a strong influence on your test or not.

For the following three modules, if the same master clock is used for the digital channel as trigger source and the analog module, you can remove this uncertainty. See *"Synchronization Uncertainty"* on page 254.

- High Speed AWG
- High Speed digitizer
- Dual High speed sampler

If the master clock used for the digital channel as trigger source is different from that used for the analog module, there is always ±1 master clock period of uncertainty.

Trigger Line Length and Signal Line Length

In addition, there are two kinds of signal delay that are caused by your wiring on a DUT board. One is the delay caused by the electrical length of the trigger line between the digital pin that provides the trigger signal and the trigger input pin of the analog module; the other is the delay caused by the electrical length of the signal line between the analog module's output/input pin and the DUT input/output pin.

Therefore, you can synchronize the digital channel operation and analog module operation by considering the following three delay factors:

- Trigger-to-signal delay of analog module
- Electric length of trigger line between digital pin and trigger input pin of analog module
- Electric length of signal line between analog module pin and DUT pin

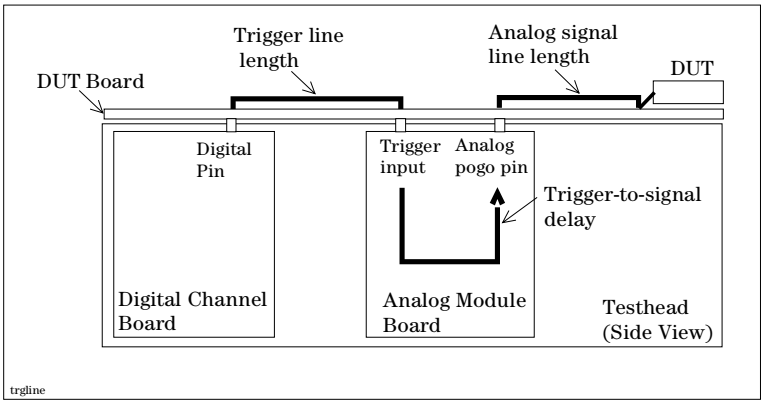


Figure 113 Delay Factors for Analog Module Operation

From these delay factors, the edge location of the trigger signal that you should set in the timing setup is decided. The following shows the timing chart for the trigger signal and analog module operation. By setting up the edge of the trigger signal as follows, the analog module can start at your desired timing.

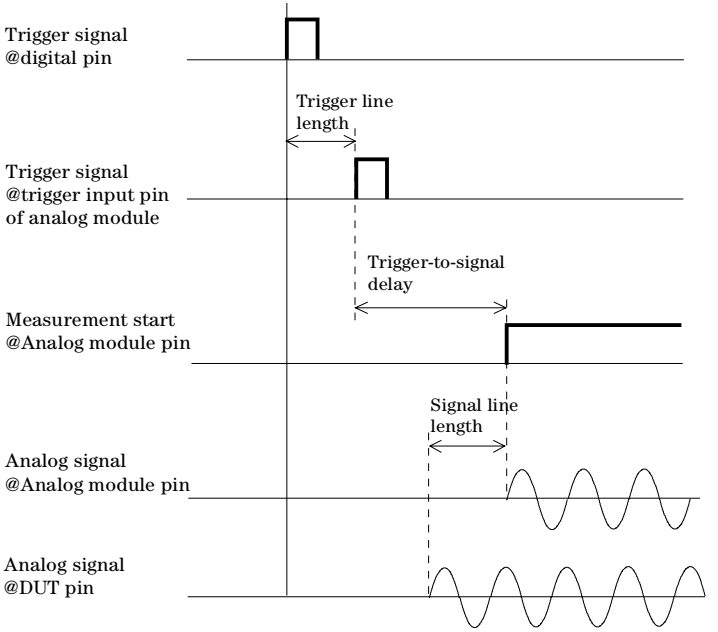


Figure 114 Timing Chart and Delay Factor

The above timing chart is an example of analog measurement.

Synchronization Categories

Required levels for accuracy of the synchronization between the digital channel operation and analog module operation depend on your application.
For example, if you want to measure analog waveform signal output from DUT regardless of the timing of digital signals to be applied to DUT, the test does not require the certainty of the synchronization. In this case, you do not have to consider these delay factors.
If you want to apply an analog waveform to a DUT with digital signals simultaneously, the test may require some certainty of the synchronization. That is, these delay factors cannot be bypassed.

The user actions for the synchronization can be categorized into the following three levels, in terms of required accuracy level. For the first level, your application needs

to consider only trigger-to-signal delay. For the second level, your application needs to consider trigger-to-signal delay, trigger line length, and signal line length. For the third level, your application uses some high speed analog modules, and needs more detailed synchronization that takes account of the synchronization uncertainty.

Currently the system software does not compensate the synchronization timing skew to account for the trigger-to-signal delay, trigger line length, and signal line length automatically. Consequently, you have to consider these delay factors to satisfy the accuracy requirement of synchronization when you program the edge location of the trigger signal. The following sections describe how you can program the edge location of the trigger signal to satisfy the required accuracy of synchronization.

- For the first level, see *"Considering Trigger-to-Signal Delay Only"* on page 249.
- For the second level, see *"Considering Trigger-to-Signal Delay, Trigger Line, and Signal Line"* on page 250.
- For the third level, see *"Considering Trigger-to-Signal Delay, Trigger Line, and Signal Line"* on page 250 and *"Synchronization Uncertainty"* on page 254.

Before going into the methods of synchronization for the three groups, the next section describes how to send a trigger signal.

Synchronization Trigger

The analog module has two pins dedicated for trigger input. One is the SYNC CLK (Synchronization Clock) pin. The other is the SYNC DATA (Synchronization Data) pin. The SYNC DATA pin is for future enhancements.

To provide a path for sending a trigger signal, connect the SYNC CLK pin to a digital channel that sends a trigger signal over one wire on the DUT board.

The pulse width of the trigger signal must be greater than or equal to 8 ns. If the pulse width of the trigger signal is smaller than 8 ns, the trigger signal may be missed by the analog module.

The input impedance of the SYNC CLK pin is 50 ohm. The threshold level of the comparator of the SYNC CLK pin is fixed to 0.0 V. The analog module activates by the rising edge of the trigger signal, that is, 0.0 V point of the rising edge. The recommended level of the trigger signal is ±500 mV (@50 ohm termination). The level of the trigger signal must be within ±1 V (@50 ohm termination).

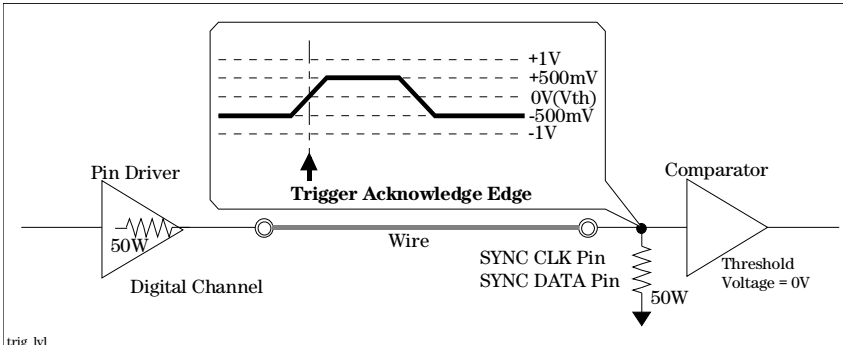


Figure 115 Synchronization Trigger

Adjusting Synchronization Timing

Considering Trigger-to-Signal Delay Only

If the trigger line delay and the signal line delay are quite smaller than the trigger-to-signal delay, you can ignore trigger line length and signal line length. Suppose you are using a digitizer to measure an analog signal from a DUT. You have to program the edge location of the trigger signal before the timing when the analog signal is output from the DUT by the trigger-to-signal delay. The following is the timing chart.

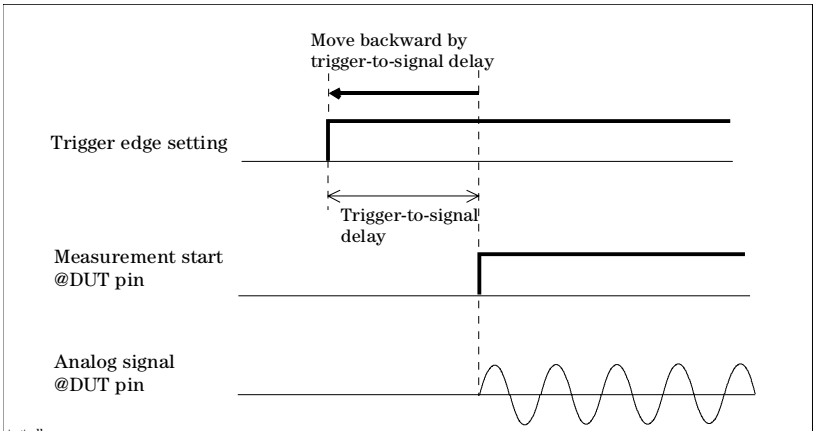


Figure 116 Adjusting Synchronization Timing (1)

Considering Trigger-to-Signal Delay, Trigger Line, and Signal Line

If you cannot ignore any delay factors in your application, you have to consider all of the following three factors:

- Trigger-to-signal delay of analog module
- Electric length of trigger line between digital pin and trigger input pin of analog module
- Electric length of signal line between analog module pin and DUT pin

For easy understanding, this section explains how to adjust timing of synchronization in two steps. The first step is about adjusting timing at the pogo pin of the analog module. The second step is about adjusting timing at the DUT pin.

Adjusting Timing at Pogo Pin of Analog Module

The following is the timing chart for measuring an analog signal from the DUT by using a digitizer. The pogo pin of the analog module is the reference point for considering timing adjustment. For the DUT, you have to stimulate it so that its analog signal can arrive at the pogo pin of the analog module at the desired measurement timing. For the digital pin that sends trigger signal, you have to program the edge location of the trigger signal before the desired measurement timing by the trigger line length plus trigger-to-signal delay. As a result, the analog signal is measured at the pogo pin of the analog module at the desired timing.

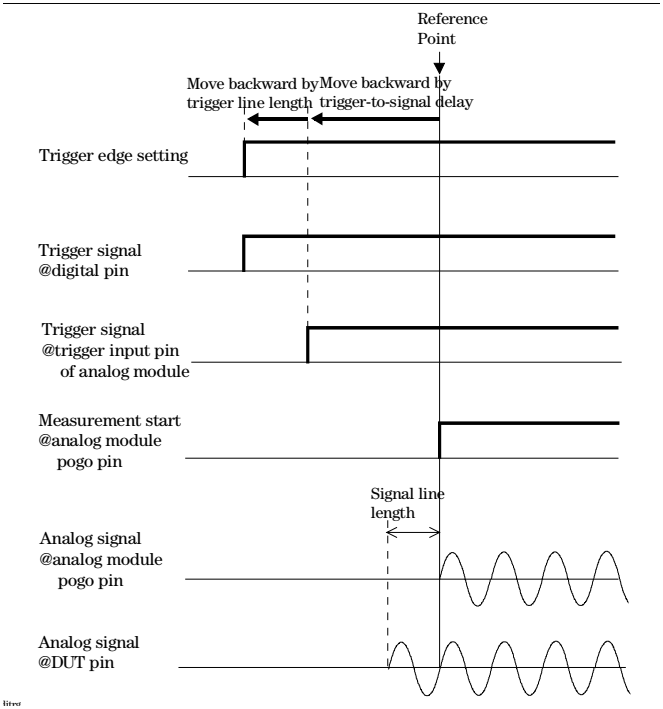


Figure 117 Adjusting Synchronization Timing (2) at Analog Module Pogo Pin

Adjusting Timing at DUT Pin

Assuming the DUT pin as the reference point of timing, you have to compensate the signal line length, which is between the DUT pin and pogo pin of the analog module, when you program the edge location of the trigger signal.

For the AWG, you have to move the trigger signal edge backward by the trigger line length plus the trigger-to-signal delay plus the signal line length from the reference point. As a result, the analog signal generated by the AWG arrives at the DUT pin at the desired timing.

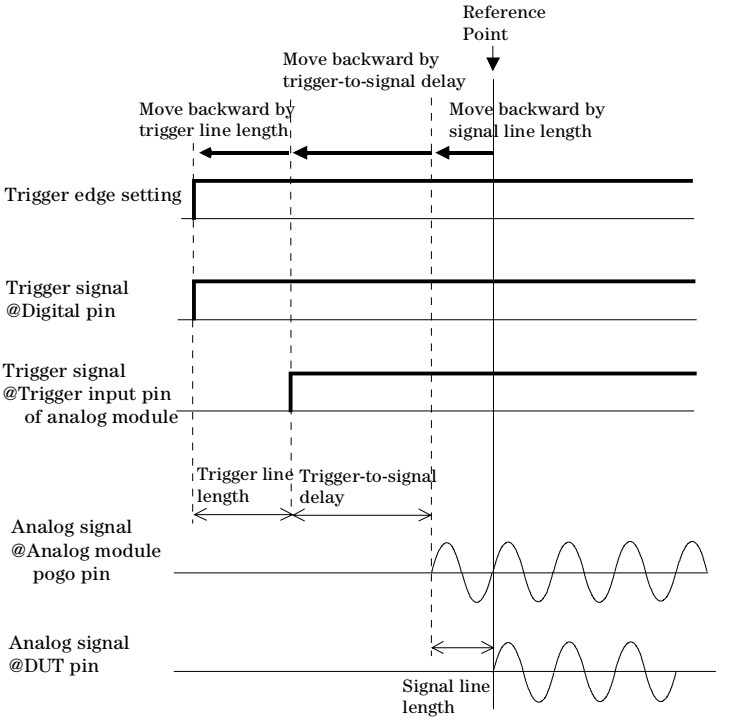


Figure 118 Adjusting Synchronization Timing (3) at DUT Pin for AWG

For a digitizer or sampler, you have to move the trigger signal edge backward by the trigger line length plus the trigger-to-signal delay from the reference point, then move it forward by the signal line length. As a result, the digitizer can start the measurement at the moment when the analog signal arrives at the analog module pin.

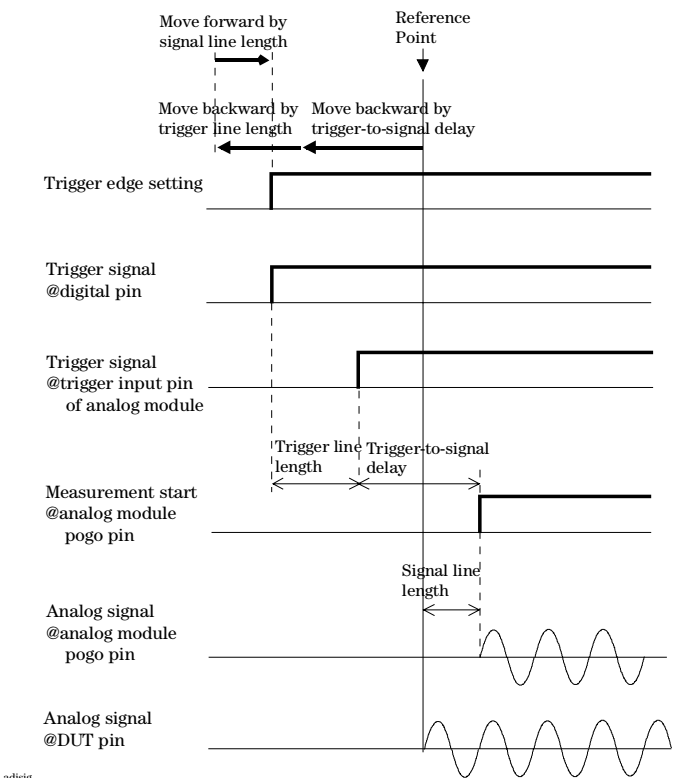


Figure 119 Adjusting Synchronization Timing (4) at DUT Pin for Digitizer and Sampler

Synchronization Uncertainty

For high speed mixed-signal applications, the key is to decrease uncertainty with the timing system in the analog modules.

The uncertainty arises from the relationship between phases of the trigger signal applied to analog modules and the master clock used for trigger signals and analog modules. Hence, uncertainty is also associated with your trigger line length on the DUT board.

For the following high speed analog modules, the timing calibration supplied by the system measures the phase between the master clock edge and the trigger edge under a fixed condition.

- High Speed AWG
- High Speed Digitizer
- Dual High Speed Sampler

Hence, the system can use the calibration data to compensate the trigger timing to the analog modules for removing the synchronization uncertainty of the timing system in the analog modules. However, this compensation is valid *only when you use the same master clock* for the digital channel as the trigger source and the analog module. This is because, when different master clocks are used for them, the phases of the master clocks are independent. Therefore, if your application requires some certainty of the synchronization, you should use the same master clock for the digital channel as is used for the trigger source and analog module.

If you use multiple analog modules when using different master clocks, uncertainty will occur between analog modules. However, you can remove *the uncertainty between the same kinds of analog modules* (for high speed AWGs or dual high speed samplers) even if you use different master clock sources for digital channels and analog modules. For details, see *"Master Trigger Function"* on page 260.

The following describes the details of how to remove the synchronization uncertainty when using same master clock for a trigger source and an analog module.

You can do either of the following to remove uncertainty that occurs in the trigger-to-signal delay of the analog module.

NOTE You can add the specified delay time value to the trigger-to-signal delay for each analog module. It is useful to adjust the edge location of the trigger signal to the desired position.

- Program the edge location of the trigger signal at the beginning of the tester period and inform the system of the trigger line length on the DUT board by using the TRGL firmware command.

  Every beginning of the tester period fully synchronizes with the master clock. At the analog module, the phase information between the master clock edge and the trigger edge is obtained by treating the beginning of the tester period as the reference point. The TRGL command calculates the difference of the trigger line length at the timing calibration and your trigger line length on the DUT board, then compensates the phase between the master clock edge and trigger edge, by treating the beginning of the tester period as the reference point. Therefore, you have to program the edge location of the trigger signal at the beginning of the tester period. The following is the timing chart.

NOTE You need to specify the trigger line length with ±200 ps (typical) accuracy in the TRGL firmware command to remove the uncertainty.

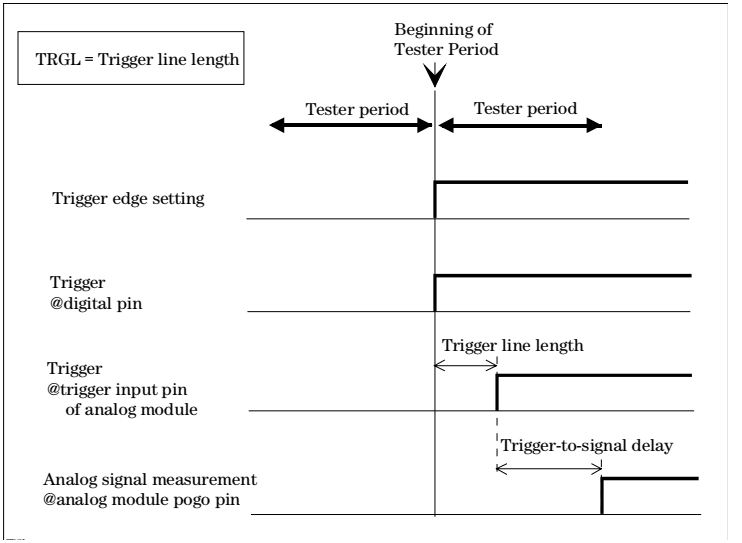


Figure 120 Trigger Signal Edge Placement when TRGL Is Set to Trigger Line Length

- Program the edge location of the trigger signal before the beginning of the tester period by the trigger line length.

  The TRGL command treats the beginning of the tester period as the reference point. Accordingly, if you program the edge timing of the trigger before the beginning of the tester period by the trigger line length, the trigger line length is virtually zero. In this case, you do not have to use the TRGL command because the default value of TRGL is zero. As well as the trigger line length setting by the TRGL command, the trigger edge setting means the system compensates the trigger timing to the analog module for removing the uncertainty automatically. The following is the timing chart.

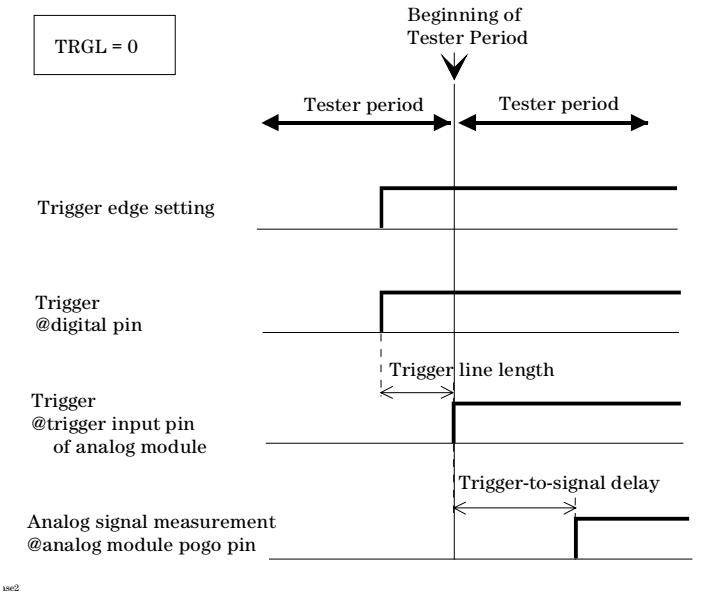


Figure 121 Trigger Signal Edge Placement when TRGL Is Set to Zero

In addition, to compensate the signal line length, which is between the analog pogo pin and DUT pin, you may want to move the edge location of the trigger signal forward by a signal line length for the case of the digitizer. You will need to inform the system of the signal line length by using the SIGL firmware command. If you do not use the SIGL command, the start timing of the analog module will be off the desired timing by the signal line length.

The following timing chart is for when the value of TRGL is set to the trigger line length.

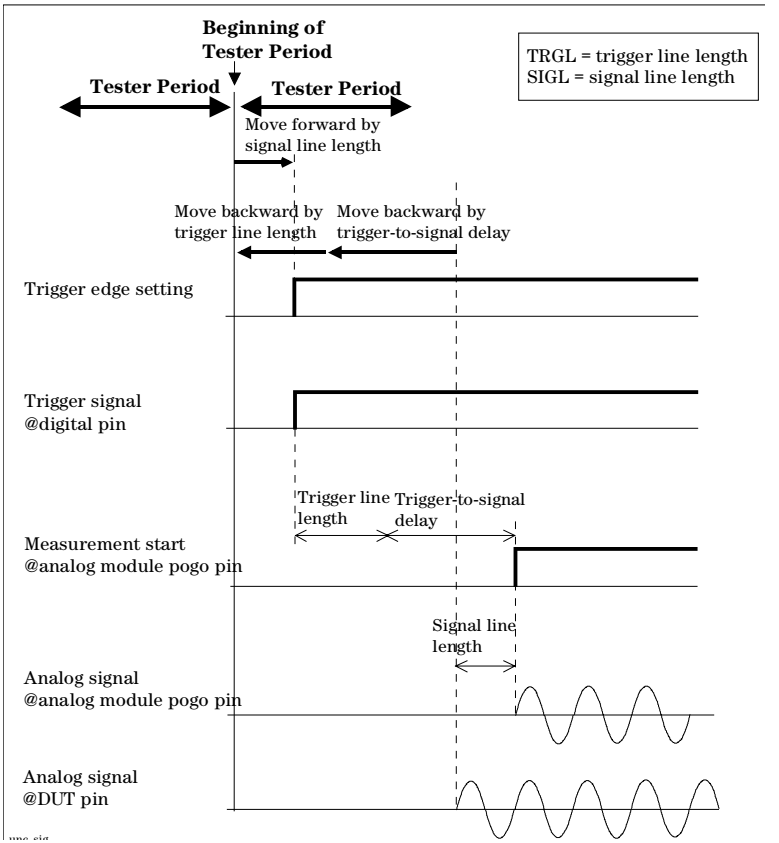


Figure 122 Trigger Signal Edge Placement when TRGL Is Set to Trigger Line Length

The following timing chart is for when the TRGL value is set to zero.

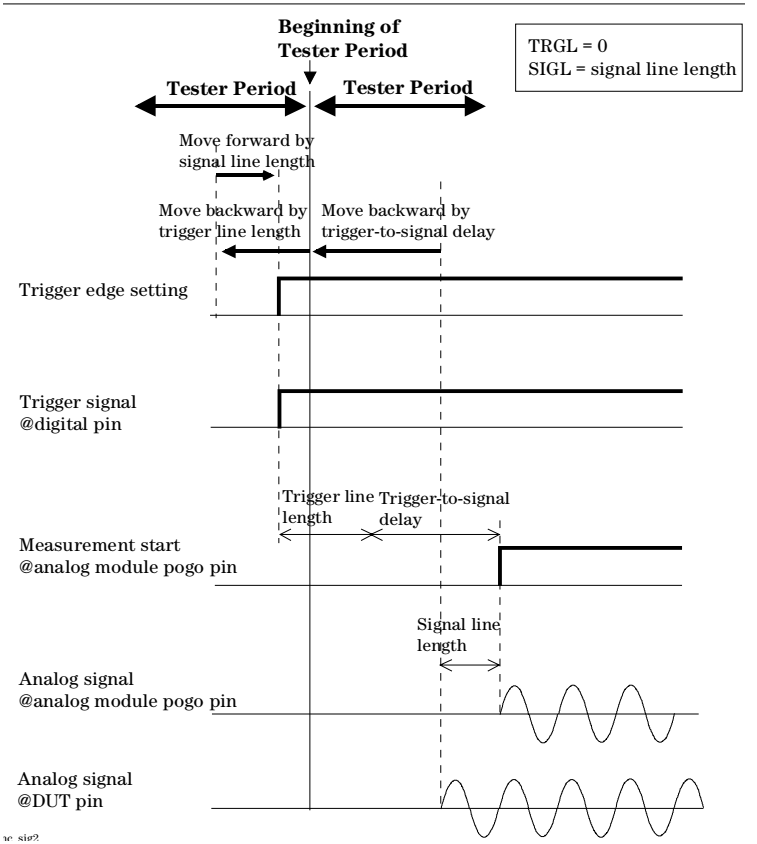


Figure 123 Trigger Signal Edge Placement when TRGL Is Set to Zero

NOTE If different master clocks are used for digital channel as trigger source and analog module, the settings of the TRGL and SIGL firmware commands are no meaning.

Master Trigger Function

When performing tests using multiple channels of high speed analog modules simultaneously, it is important to remove uncertainty between channels as much as possible.

When you use different master clock sources for digital channels and analog modules, uncertainty happens not only between the digital channels as the trigger source and analog modules, but also between analog modules. However, for High Speed AWGs and Dual High Speed Samplers, you can remove *the uncertainty between analog modules* by using the **Master Trigger Function**.

The master trigger function is available among the same kind of high speed AWGs or among dual high speed samplers. You cannot use the master trigger function among high speed AWGs and dual high speed samplers.

The master trigger function can achieve the skew between modules within ±1 ns (typical) for high speed AWGs, and ±1 ns (typical) for dual high speed samplers.

The master trigger function enables an analog module (high speed AWG or dual high speed sampler) to trigger other identical kinds of modules installed in a card cage of the testhead. For this function, all high speed AWGs or all dual high speed samplers installed in a card cage of the testhead are connected with the **"Master-Slave" internal connection**. This connection is a closed-loop in slot number order. The following figure shows the "Master-Slave" internal connection in a card cage of the testhead.

If multiple high speed AWGs or dual high speed samplers are installed in any card cage of the testhead, they are connected with the "Master-Slave" internal connection cables at the time of shipment from the factory.

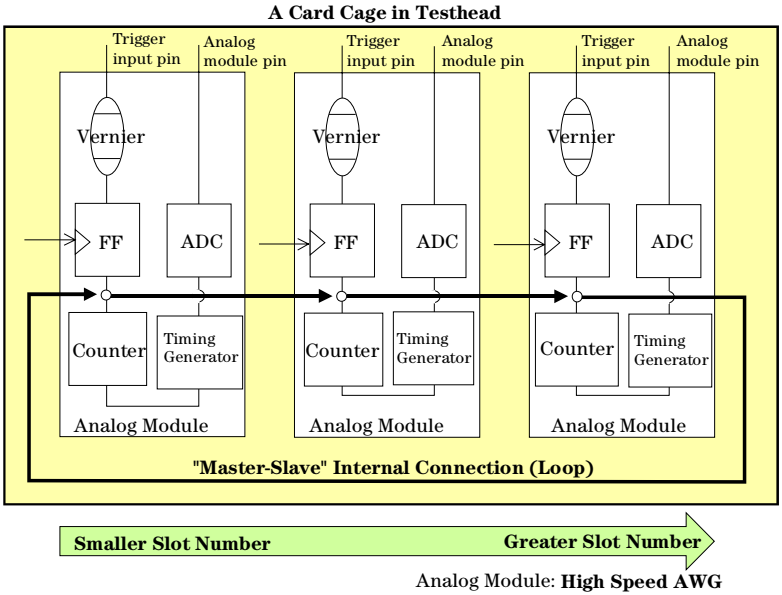


Figure 124 "Master-Slave" Internal Connections

You can define any module in the loop of the "Master-Slave" internal connection as master or slave. To define the slave module, use the ACMD "SYNM" firmware command. If you define a module as a slave module, the upstream module in the internal connection loop is defined as a master module automatically. You can get the information about the "Master-Slave" internal connection with the SOCB? firmware command. The following figure shows examples of the definition of master/slave modules.

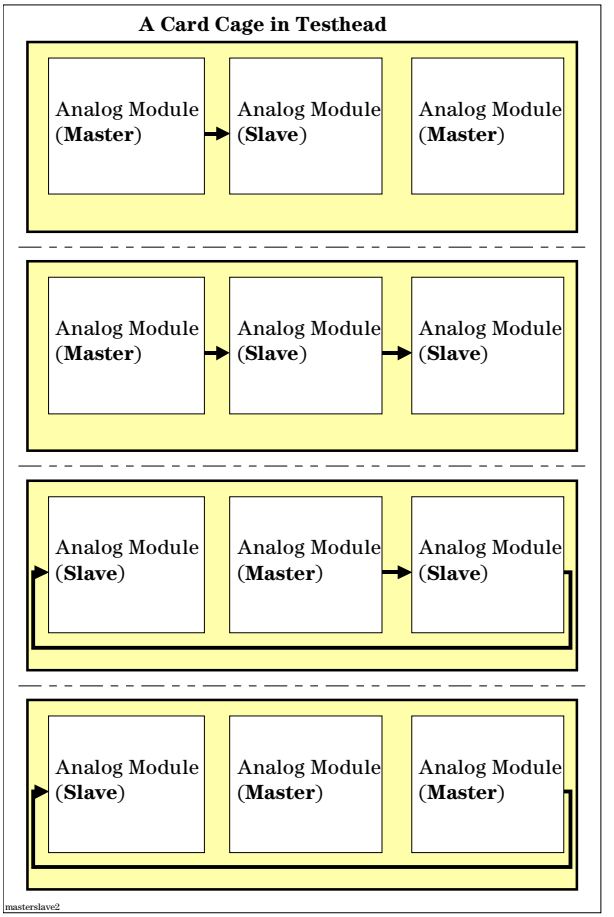


Figure 125 Examples of Definition of Master / Slave Modules

One master module can support up to seven slave modules.

The master analog module distributes the trigger that has been sampled by the master clock at the flip-flop to the slave analog modules via the "master-slave" internal connection. In the slaves, the distributed trigger signal is not sampled any more. It is input to the timing generator directly. Because the internal connection lengths between the master and the slaves are known, the system can

control the trigger-to-signal delay for the master and slaves to the same time. Hence, uncertainty between analog modules is eliminated even if you use different master clocks for digital channels and analog modules. Note that uncertainty in the trigger-to-signal delay between a digital channel and analog modules remains regardless of the use of the master trigger function.

The following figure is the block diagram for when the master trigger function is used.

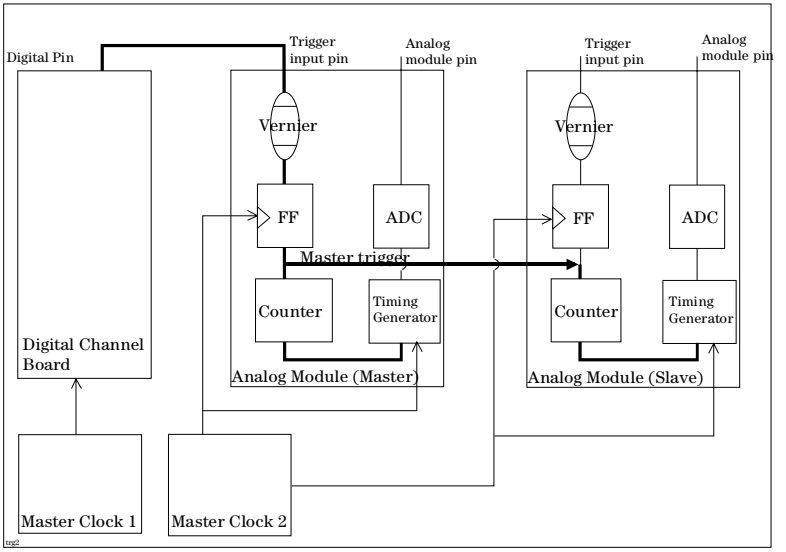


Figure 126 Master Trigger Function

Only when you use the master trigger function for the dual high speed sampler, the trigger-to-signal delay for master and slave modules changes according to the number of slave modules as follows:

Trigger-to-Signal Delay = 70 ns + (N x 15 ns)

where, N is the number of the slave modules for one master module.

For high speed AWGs, the trigger-to-signal delay for master and slave modules is always fixed to 200 ns.

Appendices

A

XICOR EEPROM Summary

On the next page you find the XICOR X24C04 EEPROM summary supplied by XICOR. This same summary is also accessible via the XICOR web-address:

www.xicor.com

Recommended System Management Alternative: X4043

XICOR

4K X24C04 512 x 8 Bit

Serial EEPROM

FEATURES

- **2.7V to 5.5V power supply versions**
- **Low power CMOS**
  - **—Active read current less than 1 mA**
  - **—Active write current less than 1.5 mA**
- **Internally organized 512 x 8**
- **2-wire serial interface**
  - **—Bidirectional data transfer protocol**
  - **—Schmitt trigger input noise suppression 400kHz across V_{CC} range**
- **Sixteen byte page write mode**
  - **—Minimizes total write time per byte**
- **Self-timed write cycle**
  - **—Typical write cycle time of 5 ms**
- **High reliability**
  - **—Endurance: 1,000,000 cycles**
  - **—Data retention: 100 years**
- **8-pin SOIC**

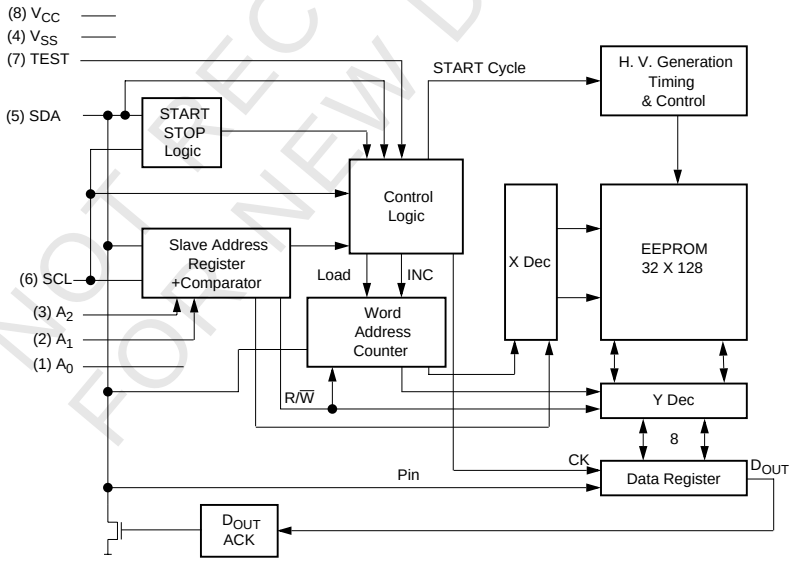
DESCRIPTION

The X24C04 is a CMOS 4096 bit serial EEPROM, internally organized 512 x 8. The X24C04 features a serial interface and software protocol allowing operation on a simple two wire bus.

The X24C04 is fabricated with Xicor's advanced CMOS Textured Poly Floating Gate Technology.

The X24C04 utilizes Xicor's proprietary DirectWrite™ cell, providing a minimum endurance of 1,000,000 cycles and a minimum data retention of 100 years.

BLOCK DIAGRAM



PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the Pull-Up Resistor selection graph at the end of this data sheet.

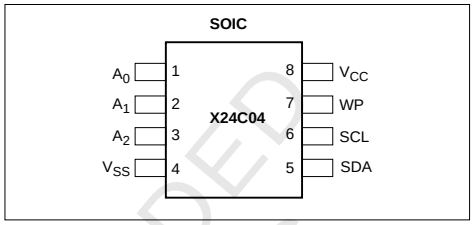
Address (A_0, A_1, A_2)

A0 is a no connect. The Address inputs (A_1, A_2) are used to set the appropriate bits of the seven bit slave address. These inputs can be used static or actively driven. If used statically they must be tied to V_{SS} or V_{CC} as appropriate. If driven they must be driven to V_{SS} or to V_{CC}.

PIN NAMES

Symbol	Description
A_0–A_2	Address Inputs
SDA	Serial Data
SCL	Serial Clock
TEST	Test Input
V_{SS}	Ground
V_{CC}	Supply Voltage

PIN CONFIGURATION



DEVICE OPERATION

The X24C04 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the X24C04 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24C04 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the X24C04 to place the device in the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

Figure 1. Data Validity

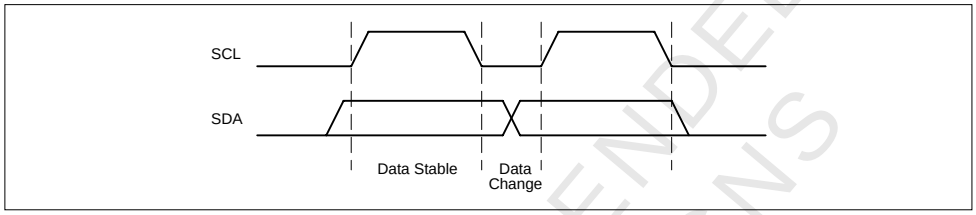
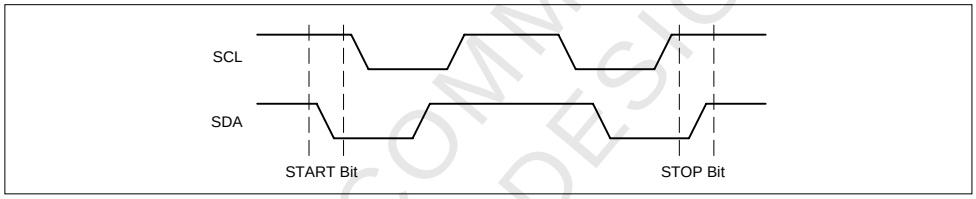


Figure 2. Definition of Start and Stop



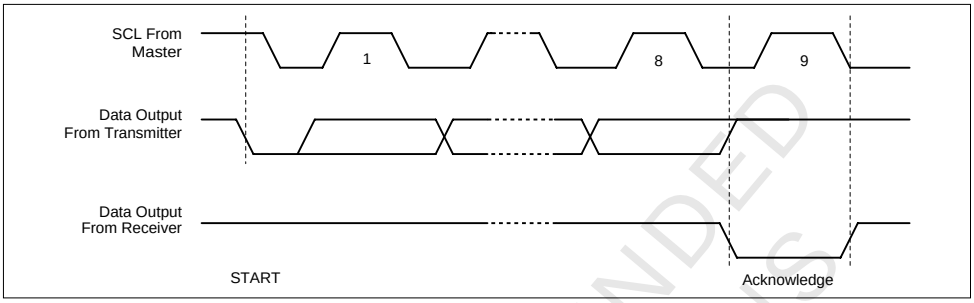
Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24C04 will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X24C04 will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the X24C04 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24C04 will continue to transmit data. If an acknowledge is not detected, the X24C04 will terminate further data transmissions. The master must then issue a stop condition to return the X24C04 to the standby power mode and place the device into a known state.

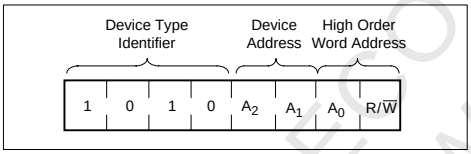
Figure 3. Acknowledge Response From Receiver



DEVICE ADDRESSING

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave are the device type identifier (see Figure 4). For the X24C04 this is fixed as 1010[B].

Figure 4. Slave Addressing



The next two significant bits address a particular device. A system could have up to four X24C04 devices on the bus (see Figure 10). The four addresses are defined by the state of the A_1 and A_2 inputs.

The next bit of the slave address is an extension of the array's address and is concatenated with the eight bits of address in the word address field, providing direct access to the whole 512 x 8 array.

Note: This bit is part of word address. Not related to device address pin A_0.

The last bit of the slave address defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected.

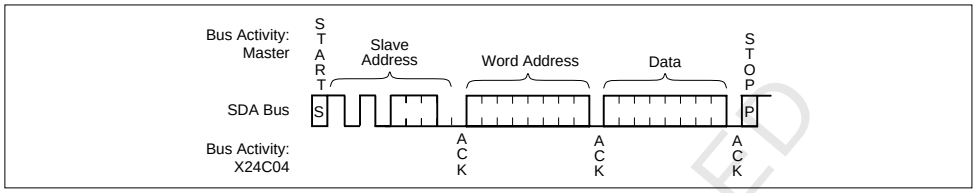
Following the start condition, the X24C04 monitors the SDA bus comparing the slave address being transmitted with its slave address (device type and state of A_1 and A_2 inputs). Upon a correct compare the X24C04 outputs an acknowledge on the SDA line. Depending on the state of the R/W bit, the X24C04 will execute a read or write operation.

WRITE OPERATIONS

Byte Write

For a write operation, the X24C04 requires a second address field. This address field is the word address, comprised of eight bits, providing access to any one of the 512 words of memory. Upon receipt of the word address the X24C04 responds with an acknowledge, and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X24C04 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the X24C04 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Figure 5. Byte Write

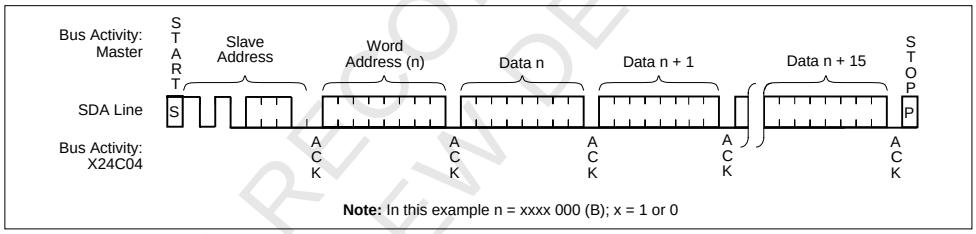


Page Write

The X24C04 is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to fifteen more words. After the receipt of each word, the X24C04 will respond with an acknowledge.

After the receipt of each word, the four low order address bits are internally incremented by one. The high order five bits of the address remain constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge and data transfer sequence.

Figure 6. Page Write

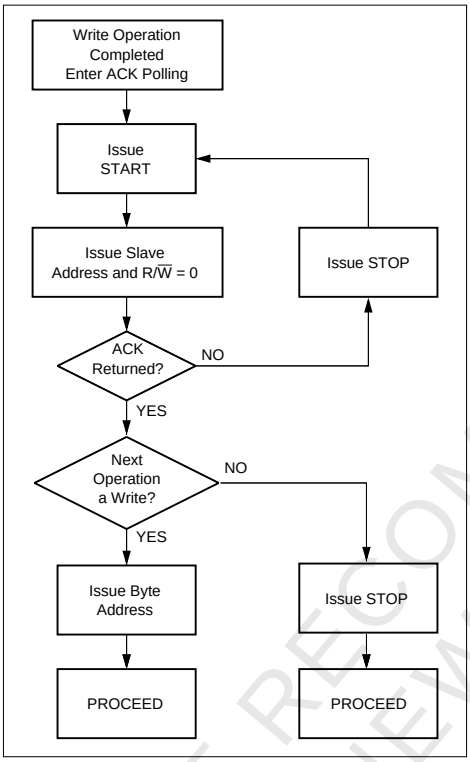


Note: In this example n = xxxx 000 (B); x = 1 or 0

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the X24C04 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition, followed by the slave address for a write operation. If the X24C04 is still busy with the write operation no ACK will be returned. If the X24C04 has completed the write operation an ACK will be returned, and the host can then proceed with the next read or write operation. Refer to Flow 1.

Flow 1. ACK Polling Sequence



READ OPERATIONS

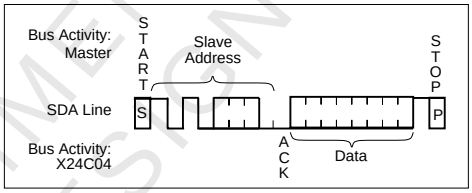
Read operations are initiated in the same manner as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

It should be noted that the ninth clock cycle of the read operation is not a “don’t care.” To terminate a read operation, the master must either issue a stop condition during the ninth cycle, or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Current Address Read

Internally the X24C04 contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with the R/$\overline{W}$ bit set to one, the X24C04 issues an acknowledge and transmits the eight bit word. The read operation is terminated by the master by not responding with an acknowledge, and issuing a stop condition. Refer to Figure 7 for the sequence of address, acknowledge and data transfer.

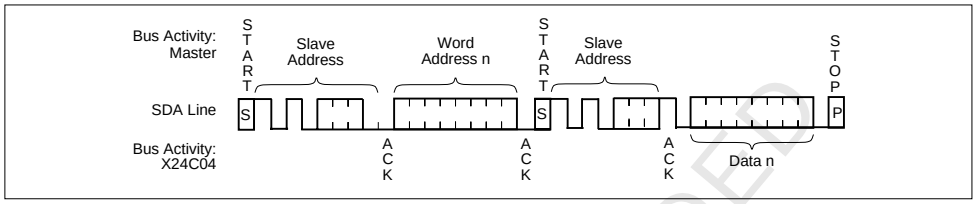
Figure 7. Current Address Read



Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a “dummy” write operation. The master issues the start condition, and the slave address followed by the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the X24C04 and then by the eight bit word. The read operation is terminated by the master by not responding with an acknowledge, and issuing a stop condition. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

Figure 8. Random Read



Sequential Read

Sequential Read can be initiated as either a current address read or random access read. The first word is transmitted as with the other modes, however, the master now responds with an acknowledge, indicating it requires additional data. The X24C04 continues to output data for each acknowledge received. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition.

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 511), the counter "rolls over" to address 0 and the X24C04 continues to output data for each acknowledge received. Refer to Figure 9 for the address, acknowledge and data transfer sequence.

Figure 9. Sequential Read

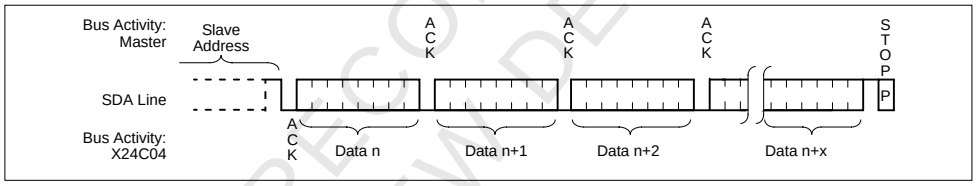
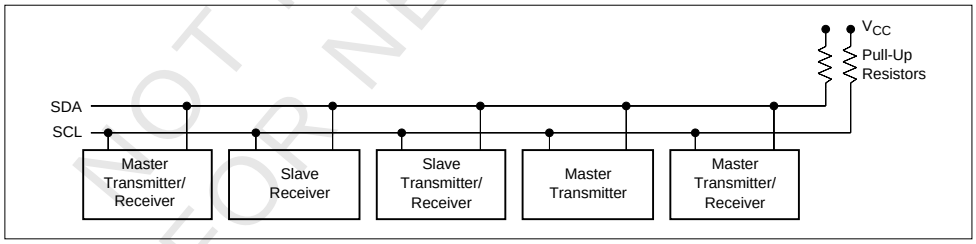


Figure 10. Typical System Configuration



ABSOLUTE MAXIMUM RATINGS

Temperature under bias .....–65 to +135°C
Storage temperature .....–65 to +150°C
Voltage on any pin with
respect to V_{SS} .....–1.0V to +7.0V
D.C. output current ..... 5 mA
Lead temperature (soldering, 10 Seconds).....300°C

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those indicated in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C

Supply Voltage	Limits
X24C04-2.7	2.7V to 5.5V

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Limits		Unit	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} supply current (Read)		1	mA	SCL = V_{CC} x 0.1/Vd x 0.9 Levels @ 100 kHz, SDA = Open, All Other Inputs = GND or V_{CC} – 0.3V
I_{CC2}	V_{CC} supply current (Write)		1.5		
$I_{SB}1$(1)	V_{CC} standby current		150	µA	SCL = SDA = V_{CC} – 0.3V, All Other Inputs = GND or V_{CC}, V_{CC} = 5.5V
I_{SB2}(1)	V_{CC} standby current		50	µA	SCL = SDA = V_{CC} – 0.3V, All Other Inputs = GND or V_{CC}, V_{CC} = 2.7V
I_{LI}	Input leakage current		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output leakage current		10	µA	V_{OUT} = GND to V_{CC}
V_{IL}(2)	Input low voltage	–1.0	V_{CC} x 0.3	V	
V_{IH}(2)	Input high voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output low voltage		0.4	V	I_{OL} = 3 mA, $V_{CC} \geq$ 2.7V

CAPACITANCE T_A = 25°C, f = 1.0MHz, V_{CC} = 5V

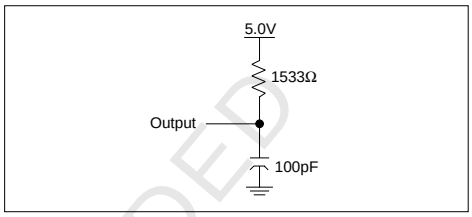
Symbol	Parameter	Max.	Unit	Test Conditions
$C_{I/O}$(3)	Input/output capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Notes: (1) Must perform a stop command prior to measurement.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(3) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input pulse levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	10 ns
Input and output timing levels	V_{CC} x 0.5

EQUIVALENT A.C. LOAD CIRCUIT



A.C. CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

Read & Write Cycle Limits

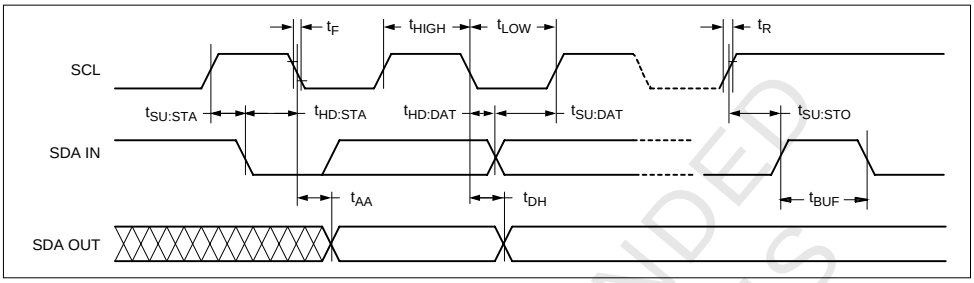
Symbol	Parameter	Min.	Max.	Unit
f_{SCL}	SCL clock frequency	0	400	kHz
T_I	Noise suppression time constant at SCL, SDA inputs	50		ns
td	SCL low to SDA data out valid	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start	1.2		µs
$t_{HD:STA}$	Start condition hold time	0.6		µs
t_{LOW}	Clock low period	1.2		µs
t_{HIGH}	Clock high period	0.6		µs
$t_{SU:STA}$	Start condition setup time (for a repeated start condition)	0.6		µs
$t_{HD:DAT}$	Data In hold time	0		µs
$t_{SU:DAT}$	Data In setup time	100		ns
t_R	SDA and SCL rise time		300	µs
t_F	SDA and SCL fall time		300	ns
$t_{SU:STO}$	Stop condition setup time	0.6		µs
t_{DH}	Data out hold time	50	300	ns

POWER-UP TIMING

Symbol	Parameter	Max.	Unit
t_{PUR}(4)	Power-up to read operation	1	ms
t_{PUW}(4)	Power-up to write operation	5	ms

Note: (4) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

Bus Timing



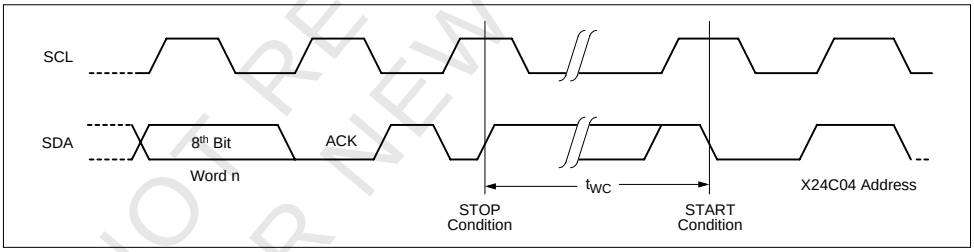
Write Cycle Limits

Symbol	Parameter	Min.	Typ.(5)	Max.	Unit
t_{WC}(6)	Write Cycle Time		5	10	ms

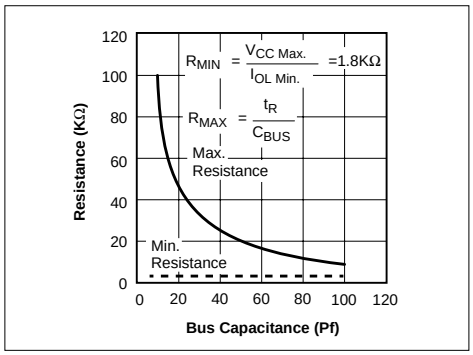
Notes: (5) Typical values are for T_A = 25°C and nominal supply voltage (5V).
(6) t_{WR} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/write cycle. During the write cycle, the X24C04 bus interface circuits are disabled, SDA is allowed to remain HIGH, and the device does not respond to its slave address.

Write Cycle Timing



Guidelines for Calculating Typical Values of Bus Pull-Up Resistors

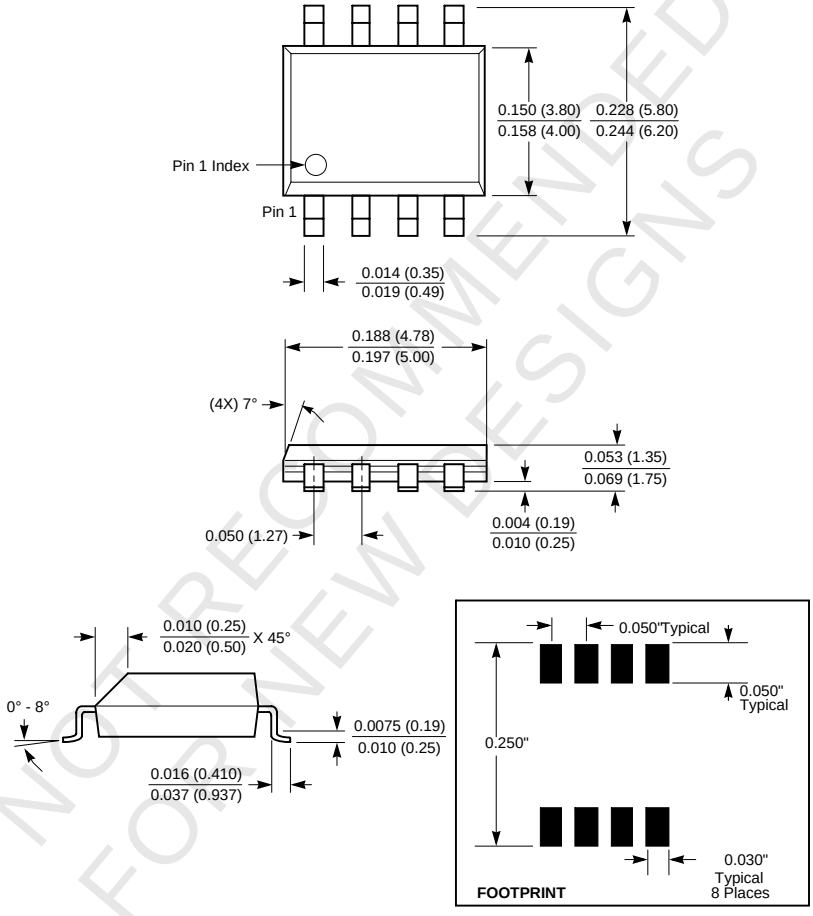


SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

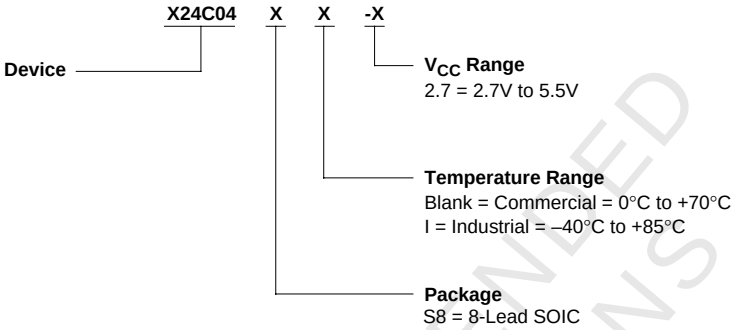
PACKAGING INFORMATION

8-Lead Plastic Small Outline Gull Wing Package Type S

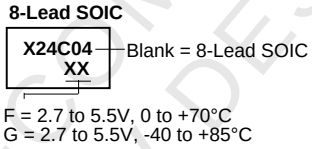


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

Ordering Information



Part Mark Convention



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